

5IW / 5IS

(VER. 1.x) / (VER. 3.x)

SYSTEM BOARD

OPERATION MANUAL

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Edition : 1.0

TRADEMARKS

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NOTE

The "LOAD SETUP DEFAULTS" function loads the default settings directly from BIOS default table, these default settings are the best-case values that should optimize system performance. This function will be necessary when you accept this system board, or the system CMOS data is corrupted.

By pressing "Enter" key, while "LOAD SETUP DEFAULTS" is highlighted, then presses "Y" and "Enter" key. the SETUP default values will be loaded. (Please refer to the Chapter 5 AWARD BIOS SETUP procedures in this manual.)

1. INTRODUCTION

1.1 SYSTEM OVERVIEW

The 5IW /5IS Pentium PCI Local Bus system board is a "half-all-in-one" system board. It is designed based on the Intel 82430FX PCIset system chipset and Winbond / SMC (or UMC) I/O chipset, which built-in two channels PIO and Bus Master PCI IDE port, one Floppy Disk control port, two high speed Serial ports (UARTs) and one multimode Parallel prot. This system board is designed to fit a high performance, Pentium 75 MHz to 200 MHz (ideally) based solution for high-end and true GREEN-PC computer systems. This system board supports the Peripheral Component Interconnect (PCI) Local Bus standard (Rev. 2.0). It not only breaks through the I/O bottlenecks of the traditional ISA main board, but also provides the performance needs for networking and multi-user environments.

1.2 FEATURES

The 5IW / 5IS system board supports the following features:

- Pentium P54C/P54CT/P54CS/P55C/P55CT based, PC/AT compatible system board with ISA Bus and PCI Local Bus.
- Supports the most part Pentium and OverDrive CPUs designed and manufactured by Intel.
- Built-in 2 sets voltage regulator circuit to support multi-spec. CPU I/O voltage (includes Standard, VR and VRE specification) and CPU CORE voltage (+2.5V DC).
- Supports true GREEN function.
- DRAM Memory : Supports both standard fast page(FP) mode and Extended Data Out (EDO).
- Cache Memory : Supports either burst, pipelined burst or standard (asynchronous) SRAMs.
- Shadow RAM : Supports shadow RAM for system, video and optional adapter BIOS.
- BIOS : Supports Plug and Play BIOS.
- IDE ports : Supports two channels PIO and Bus Master PCI IDE port, up to Mode 4 timing, and up to 22 MBytes/s transfer rates.
- I/O ports : Supports two high speed serial ports (UARTs), One multimode parallel port for standard (Normal/SPP), enhanced (EPP) and high speed (ECP) modes. One Floppy Disk Control port.
- IR Port (option) : Supports IR (Infrared Rays) functions. Both HPSIR and ASKIR are supported. (Supported, only when the I/O chip is used Winbond W83877F, SMC FDC37C665IR/FDC37C669 or UMC UM8669F).
- Software compatibility : MS-DOS, WindowsNT, OS2, XENIX, UNIX, NOVELL, CAD/CAM, Windows, Windows 95....etc.

2. SPECIFICATIONS

- CPU**
Intel Pentium processor and OverDrive processor (P54C/P54CT/P54CS/P55C/P55CT)
75/90/100/120/133 MHz and 150/166/180/200 MHz. (ideally)
- CPU VCC**
(1). CPU I/O voltage : Supports Standard, VR and VRE specification.
(2). CPU CORE voltage : Supports both "equal to CPU I/O voltage" and "+2.5V DC"
- WORD SIZE**
Data Path : 8-bit, 16-bit, 32-bit, 64-bit
- PC System Chipset**
Intel 82430FX PCIset (82437FX, 82438FX, 82371FB)
- I/O Chipset**
5IW : Winbond W83787F / W83787IF / W83877F
5IS : SMC FDC37C665GT / FDC37C665IR / FDC37C669 or UMC UM8669F.
- System Clock**
50/60/66.6 MHz adjustable.
- Memory**
DRAM : Two banks, each bank could be single or double sided, 8MB up to 128 MB.
Supports both standard fast page (FP) mode and Extended Data Out (EDO) memory.
SRAM : (1). Asynchronous SRAMs and Burst SRAMs
One bank, 256KB/512KB, supports by SRAM module.
(2). Pipeline-burst SRAMs
Two banks, 256KB/512KB, supports by onboard direct-mounted and (or)
SRAM module.
- BIOS**
AWARD or AMI System BIOS. 128KBx8, Flash ROM. (Plug & Play BIOS)
- Expansion Slots**
PCI Slots : 32-bit x 4 (All Master/Slave)
ISA Slots : 16-bit x 4
- IDE Ports**
Two channels PIO and Bus Master PCI IDE port, maximum could be connected 4 IDE Hard
Disk and ATAPI CD-ROM device.

- Super I/O Ports**
 1. Two high speed NS16C550 compatible serial ports (UARTs).
 2. One parallel port, supports Normal(SPP)/EPP/ECP mode.
 3. One Floppy Disk Control port.

- IR Port (option)**

One HPSIR and ASKIR compatible IR transmission connector (4-pin).

- Mouse and Keyboard**

Supports PS/2 Mouse connector (option), PS/2 Keyboard connector (option) and AT Keyboard connector.

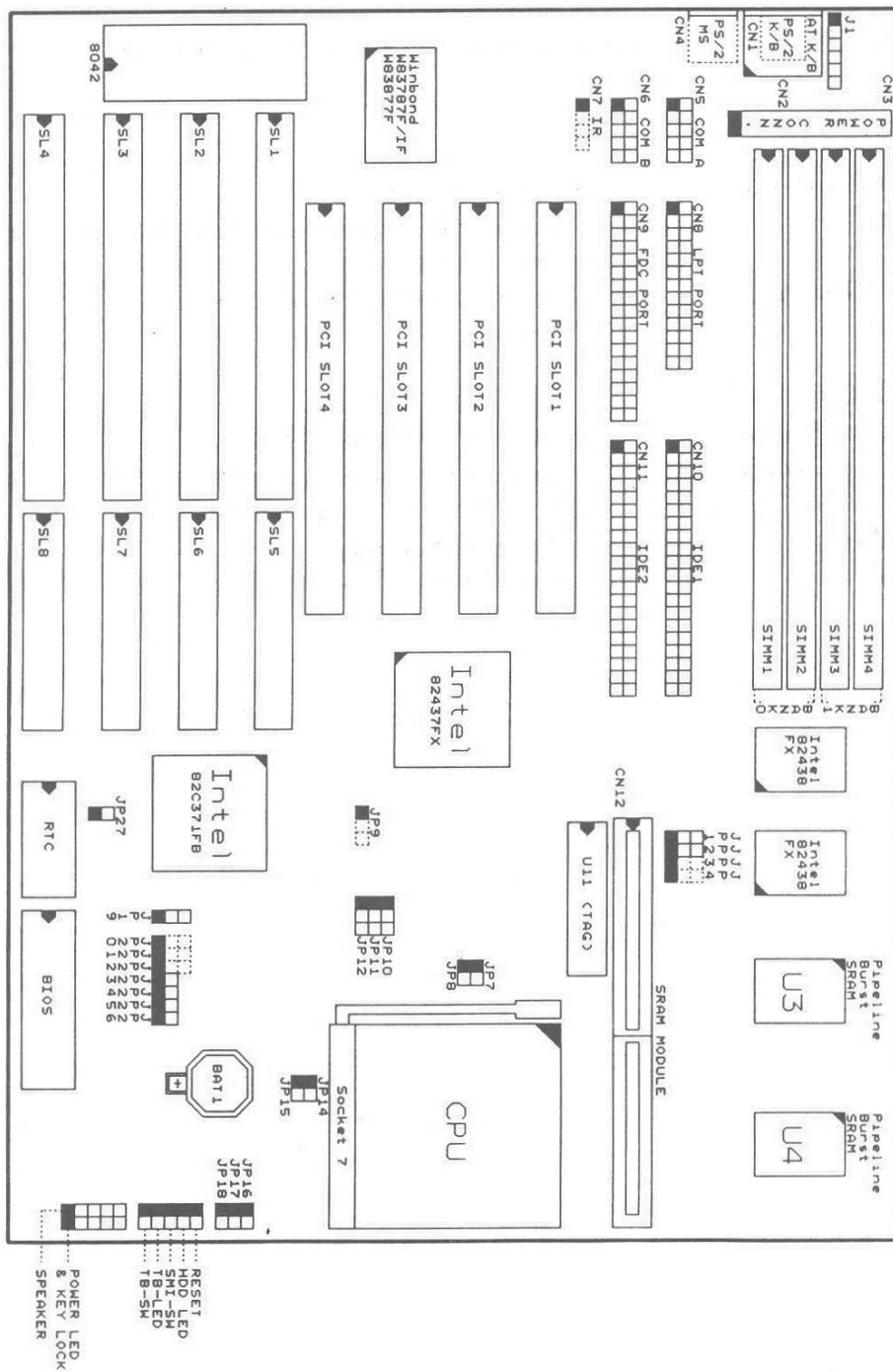
- DIMENSION**
 - Width & Length** : 220 mm x 290 mm.
 - Height** : 3/4 inches with components mounted, but without expansion boards and cables.
 - PCB Thickness** : 4 layers, 0.05 inches normal.
 - Weight** : 21.5 ounces.

- ENVIRONMENT**
 - Operating Temperature** : 10°C to 40°C. (50°F to 104°F)
 - Required Airflow** : 50 linear feet per minute across 80486 CPU.
 - Storage Temperature** : - 40°C to 70°C. (- 40°F to 158°F)
 - Humidity** : 0 to 90% noncondensing.
 - Altitude** : 0 to 10,000 feet.

3. SYSTEM BOARD LAYOUT

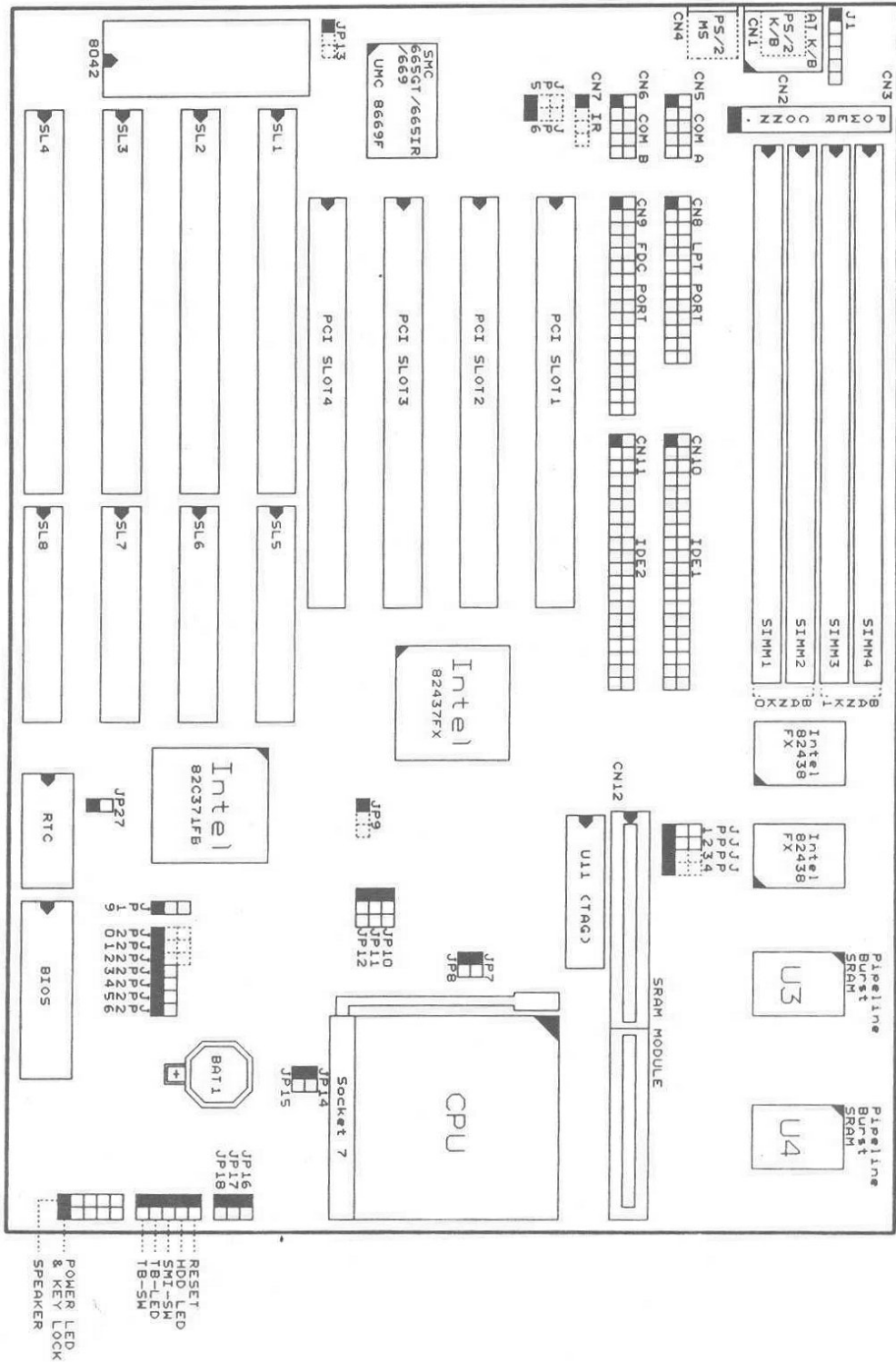
3.1 5IW Ver. 1.0

Explanation : All connectors, jumpers and components which marks by a black point on the corner means the Pin-1 side of the connector, jumper and component.



3.2 5IS Ver. 3.0

Explanation : All connectors, jumpers and components which marks by a black point on the corner means the Pin-1 side of the connector, jumper and component.



4. HARDWARE SETUP

4.1 UNPACKING

The system board package should contain the following parts :

- The 5IW / 5IS system board.
- OPERATION MANUAL.
- Cable set for IDE and I/O device.

4.2 HARDWARE CONFIGURATION

Before the system board is ready to operate, the hardware must be configured to allow for various functions within the system. To configure the 5IW / 5IS system board is a simple task, only a few jumpers, connectors, cables and sockets needs to be selected and installed. For the detailed locations of each component please refer to the system board layout figure which appears in page 3-1 (5IW), and page 3-2 (5IS)

4.2.1 DRAM INSTALLATION

The 5IW / 5IS system board will support two banks main memory (bank0 and bank 1) on board, (using four 72-Pin SIMM socket, SIMM 1 - 4), each bank could be single or double sided. With the use of 1MBx36(32)-S, 2MBx36(32)-D, 4MBx36(32)-S or 8MBx36(32)-D SIMM modules, 8MB up to 128 MB of local memory can be attained. Both standard fast page (FP) mode and Extended Data Out (EDO) memory are supported, but they cannot be mixed within the same memory bank. The speed of FP DRAMs must be used 70ns or faster than 70ns and the speed of EDO DRAMs must be used 60ns or faster than 60ns. (Note :S = Single sided , D = Double sided)

There are no jumper needed for DRAM configuration, DRAMs' type and size will be detected by system BIOS automatically, the following table provides all possible memory combination.

Total Size	Bank 0	Bank 1	Total Size	Bank 0	Bank 1
	SIMM1, SIMM2	SIMM3, SIMM4		SIMM1, SIMM2	SIMM3, SIMM4
8 MB	1MBx36(32)-S	Empty	32 MB	4MBx36(32)-S	Empty
16 MB	1MBx36(32)-S	1MBx36(32)-S	40 MB	4MBx36(32)-S	1MBx36(32)-S
24 MB	1MBx36(32)-S	2MBx36(32)-D	48 MB	4MBx36(32)-S	2MBx36(32)-D
40 MB	1MBx36(32)-S	4MBx36(32)-S	64 MB	4MBx36(32)-S	4MBx36(32)-S
72 MB	1MBx36(32)-S	8MBx36(32)-D	96 MB	4MBx36(32)-S	8MBx36(32)-D
16 MB	2MBx36(32)-D	Empty	64 MB	8MBx36(32)-D	Empty
24 MB	2MBx36(32)-D	1MBx36(32)-S	72 MB	8MBx36(32)-D	1MBx36(32)-S
32 MB	2MBx36(32)-D	2MBx36(32)-D	80 MB	8MBx36(32)-D	2MBx36(32)-D
48 MB	2MBx36(32)-D	4MBx36(32)-S	96 MB	8MBx36(32)-D	4MBx36(32)-S
80 MB	2MBx36(32)-D	8MBx36(32)-D	128 MB	8MBx36(32)-D	8MBx36(32)-D

4.2.2 CACHE MEMORY INSTALLATION AND JUMPER SETUP

The 5IW (Ver. 1.x) / 5IS (Ver. 3.x) system board is designed to fit the pipeline-burst SRAMs mainly, but also supports burst SRAMs and asynchronous SRAMs, it will support one or two bank(s) direct-mapped L2 cache memory and provides either 256KB or 512KB cache memory size, both Write Back and Write Through cache update policy are supported. The pipeline-burst SRAMs are supported by "onboard direct-mounted", and (or) "a 160-pin slot and a special SRAMs modules". The burst SRAMs and standard (asynchronous) SRAMs are supported by the special SRAMs modules.

- Note :*
1. The SRAMs modules design (includes pipeline-burst, burst and asynchronous) must comply with Intel COASt (Cache-On-A-Stick) module specification revision 1.2 or later.
 2. The 5IW / 5IS system board supports just one type of L2 cache memory (pipeline-burst, burst or asynchronous SRAMs) at the same time, mean that you could not mixed use the different type SRAMs at the same time.

4.2.2.1 PIPELINE-BURST SRAMs CACHE MEMORY CONFIGURATION

The 5IW (Ver. 1.x) / 5IS (Ver. 3.x) system board will support one or two bank(s) pipeline-burst SRAMs cache memory. They are supported by "onboard direct-mounted", and (or) "SRAMs modules". The cache size could be upgraded from 256KB to 512KB while uses both "onboard direct-mounted SRAMs" and "SRAMs modules". The following table lists the jumper settings while uses pipeline-burst SRAMs cache memory.

JP1	JP2	Remark
2-3	2-3	default

4.2.2.2 BURST SRAMs CACHE MEMORY CONFIGURATION

The 5IW (Ver. 1.x) / 5IS (Ver. 3.x) system board will support one bank burst SRAMs cache memory. They are supported by "SRAMs modules". The following table lists the jumper settings while uses "burst SRAMs modules" cache memory .

JP1	JP2	Remark
2-3	2-3	Removed all onboard pipeline-burst SRAMs (U3, U4) and TAG SRAM (U11)

4.2.2.3 ASYNCHRONOUS SRAMs CACHE MEMORY CONFIGURATION

The 5IW (Ver. 1.x) / 5IS (Ver. 3.x) system board will support one bank asynchronous SRAMs cache memory. They are supported by "SRAMs modules". The following table lists the jumper settings while uses "asynchronous SRAMs modules" cache memory.

JP1	JP2	Remark
1-2	1-2	Removed all onboard pipeline-burst SRAMs (U3, U4) and TAG SRAM (U11)

4.2.3 CONNECTORS

A connector is two or more pins that are used make connections to the system standard accessories (such as power, mouse, printer,...etc.) The following is a list of connectors on board, as well as descriptions of each individual connector.

(A) BAT1 Non-Rechargeable battery (Using 3 Vlots Lithium battery : CR2032)

<u>Pin #</u>	<u>Assignment</u>
<input type="checkbox"/>	Battery Positive
<input type="checkbox"/>	Ground

(B) CN1 PS/2 Keyboard connector (option)

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	Keyboard Data	4	+5V DC
2	No Connection	5	Keyboard Clock
3	Ground	6	No Connection

(C) CN2 AT Keyboard connector

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	Keyboard Clock	4	Ground
2	Keyboard Data	5	+5V DC
3	No Connection		

(D) CN3 Power connector

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	Power Good	5	Ground	9	-5V DC
2	+5V DC	6	Ground	10	+5V DC
3	+12V DC	7	Ground	11	+5V DC
4	-12V DC	8	Ground	12	+5V DC

(E) CN4 PS/2 Mouse connector (option) & J1 PS/2 Mouse converted connector

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	Mouse Data	1	Mouse Data
2	No Connection	2	No Connection
3	Ground	3	Ground
4	+5V DC	4	+5V DC
5	Mouse Clock	5	Mouse Clock
6	No Connection	6	No Connection

(F) CN5 COM A (Serial Port 1) connector

- 5IW : COM1/3/4, selected by BIOS setup, using IRQ4 or 3
- 5IS : COM1/2/3/4, selected by BIOS setup, using IRQ4 or 3

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	DCD (Data Carrier Detect)	2	RD (Received Data)
3	TD (Transmit Data)	4	DTR (Data Terminal Ready)
5	Ground	6	DSR (Data Set Ready)
7	RTS (Request To Send)	8	CTS (Clear To Send)
9	RI (Ring Indicator)	10	NC (No Connection)

(G) CN6 COM B (Serial Port 2) connector

1. 5IW : COM2/3/4, selected by BIOS setup, using IRQ3 or 4
2. 5IS : COM1/2/3/4, selected by BIOS setup, using IRQ3 or 4

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	DCD (Data Carrier Detect)	2	RD (Received Data)
3	TD (Transmit Data)	4	DTR (Data Terminal Ready)
5	Ground	6	DSR (Data Set Ready)
7	RTS (Request To Send)	8	CTS (Clear To Send)
9	RI (Ring Indicator)	10	NC (No Connection)

(H) CN7 IR (Infrared Rays) transmission connector

Available, only when the I/O Chip is used :

1. 5IW : Winbond W83C877F
2. 5IS : SMC FDC37C665IR/FDC37C669 or UMC UM8669F

If the other I/O chip is used, the IR functions are not supported and this connector is removed.

<u>Pin #</u>	<u>Assignment</u>	<u>Pin #</u>	<u>Assignment</u>
1	IR Receive	3	IR Transmit
2	Ground	4	+5V DC

(I) CN8 Parallel Port connector

Supports Normal(SPP)/EPP/ECP mode, selected by BIOS setup,

1. 5IW : Using IRQ7, ECP using DMA channel 3
2. 5IS : (i) SMC I/O : Using IRQ7, ECP using DMA channel 3
(ii) UMC I/O : Using IRQ7 or 5, ECP using DMA channel 1 or 3

(J) CN9 Floppy Disk Control Port connector (Using IRQ6, DMA channel 2)

(K) CN10 IDE 1 connector (Primary IDE Port, using IRQ14)

(L) CN11 IDE 2 connector (Secondary IDE Port, using MIRQ0)

(M) CN12 SRAM module slot

(N) RS Reset Button connector

<u>Pin #</u>	<u>Assignment</u>	<u>Pin1&2</u>	<u>Function</u>
1	Ground	Open	No action
2	Reset Control	Short	Reset

(O) HL IDE HDD LED connector

<u>Pin #</u>	<u>Assignment</u>
1	Pullup (+5V DC)
2	Signal Pin

- (P) SS External SMI button connector
- | <u>Pin #</u> | <u>Assignment</u> | <u>Pin1&2</u> | <u>Function</u> |
|--------------|-------------------|-------------------|--------------------------|
| 1 | SMI Control | Open | For normal operation |
| 2 | Ground | Short | To get into Suspend mode |
- (Q) TL Turbo LED connector
- | <u>Pin #</u> | <u>Assignment</u> |
|--------------|-------------------|
| 1 | Pullup (+5V DC) |
| 2 | Signal Pin |
- (R) TS Turbo Switch connector (This function is reserved)
- | <u>Pin #</u> | <u>Assignment</u> | <u>Pin1&2</u> | <u>Function</u> |
|--------------|-------------------|-------------------|-----------------|
| 1 | Ground | Open | Turbo |
| 2 | Turbo Control | Short | Normal |
- (S) SPEAKER Speaker connector
- | <u>Pin #</u> | <u>Assignment</u> | <u>Pin #</u> | <u>Assignmen</u> |
|--------------|-------------------|--------------|---------------------|
| 1 | +5V DC | 4 | Speaker Data Signal |
| 2 | No Connection | 5 | No Connection |
| 3 | No Connection | | |
- (T) KEY LOCK Front Panal Power LED & Key-Lock connector
- | <u>Pin #</u> | <u>Assignment</u> |
|--------------|-------------------------------|
| 1 | Pullup (+5V DC for Power LED) |
| 2 | No Connection |
| 3 | Ground |
| 4 | Keyboard Lock |
| 5 | Ground |

4.2.4 JUMPERS

A jumper is two, three or more pins which may or may not be covered by a plastic connector plug (mini-jumper). A jumper is used to select different system options. **Please make sure all jumpers at correct position before this system board used.**

(A) JP1, JP2 Cache memory configuration

Please refer to page 4-2 for detailed informations.

(B) JP3, JP4 (Reserved)

(C) JP5, JP6 IR Function selection (For 5IS only)

Availablely, only when the I/O chip is used SMC FDC37C665IR(B). If the I/O chip is used SMC FDC37C665IR(C) / FDC37C665GT / FDC37C669 or UMC UM866, these pin-connector and mini-jumper are removed and the settings are fixed on 1-2.

Pin # Function

1-2 Enable COM B (CN6, Serial Port 2) function and Disable IR (CN7) function.

2-3 Disable COM B (CN6, Serial Port 2) function and Enable IR (CN7) function.

(D) JP16, JP17, JP18 CPU I/O voltage selection

CPU I/O voltage	JP16	JP17	JP18	Remark
+ 3.3 V	open	open	short	For standard spec. CPUs (default)
+ 3.4 V	open	short	open	For VR spec. CPUs
+ 3.5 V	short	open	open	For VRE spec. CPUs

(E) JP7, JP8, JP14, JP15 CPU CORE voltage selection

CPU CORE voltage	JP7, JP8	JP14, JP15	Remark
Equal to CPU I/O voltage	open, open	short, short	For P54 (default)
+ 2.5 V	short, short	open, open	For P55

(F) JP10, JP11, JP12 Frequency selection

The clock generator IC (U13) used on this system board maybe two types, there are a few different jumper-settings between them, before these jumpers adjusted, please check the type of U13 first, then adjusted them according to the following two tables.

(1) If the clock generator IC (U13) is pin-to-pin compatible with IC WORKS 48C60-402G

Frequency (unit : MHz)						Remark
System	PCI Bus	AT Bus	JP10	JP11	JP12	(CPU Type)
50	25	8.33	2-3	2-3	1-2	For P5-75, 6x86-100
60	30	7.5	2-3	open	2-3	For P5-90/120/150/180, 6x86-120 (default)
66.6	33.3	8.33	open	2-3	2-3	For P5-100/133/166/200, 6x86-133

(2) If the clock generator IC (U13) is pin-to-pin compatible with IMI SC498AXB

Frequency (unit : MHz)						Remark
System	PCI Bus	AT Bus	JP10	JP11	JP12	(CPU Type)
50	25	8.33	open	open	1-2	For P5-75, 6x86-100
60	30	7.5	open	1-2	2-3	For P5-90/120/150/180, 6x86-120 (default)
66.6	33.3	8.33	1-2	open	2-3	For P5-100/133/166/200, 6x86-133

(G) JP25, JP26 CPU-to-System Frequency ratio selection

Ratio	JP25	JP26	Remark (CPU Type)
3/2 (x 1.5)	open	open	For P5-75/90/100 (default)
2/1 (x 2)	short	open	For P5-120/133, 6x86-100/120/133
5/2 (x 2.5)	short	short	For P5-150/166
3/1 (x 3)	open	short	For P5-180/200

(H) JP9 Clock generator VCC voltage selection

<u>Pin #</u>	<u>Function</u>
1-2	+ 5V (default)
2-3	+ 3.3V

(I) JP19 ROM BIOS Selection

<u>Pin #</u>	<u>Function</u>
1-2	For +5V FLASH ROM, EPROM
2-3	For +12V FLASH ROM

(J) JP23 CPU Internal Cache (L1) Write Back / Write Through selection

<u>Pin #</u>	<u>Function</u>
open	CPU Internal Cache Write Back (default)
short	CPU Internal Cache Write Through

(K) JP24 CPU Pipelined function selection

<u>Pin #</u>	<u>Function</u>
open	CPU Pipelined Disable
short	CPU Pipelined Enable (Default)

(L) JP27 CMOS Discharge button

<u>Pin #</u>	<u>Function</u>
open	Normal operation
short	CMOS Discharge

5. AWARD BIOS SETUP

5.1 GETTING STARTED

When the system is first powered on or reset, the BIOS will enter the Power-On Self Test routines (POST : Display a copyright message on the first line of the screen followed by a diagnostics and initialization procedure.) (If an EGA or VGA card is installed, the copyright message of the video card maybe displayed on the screen first.) The BIOS will indicate any error or malfunction by a series of beeps or display the error message on screen.

Normally, the simulate figure 5-1 will display on the screen when the system is powered on.

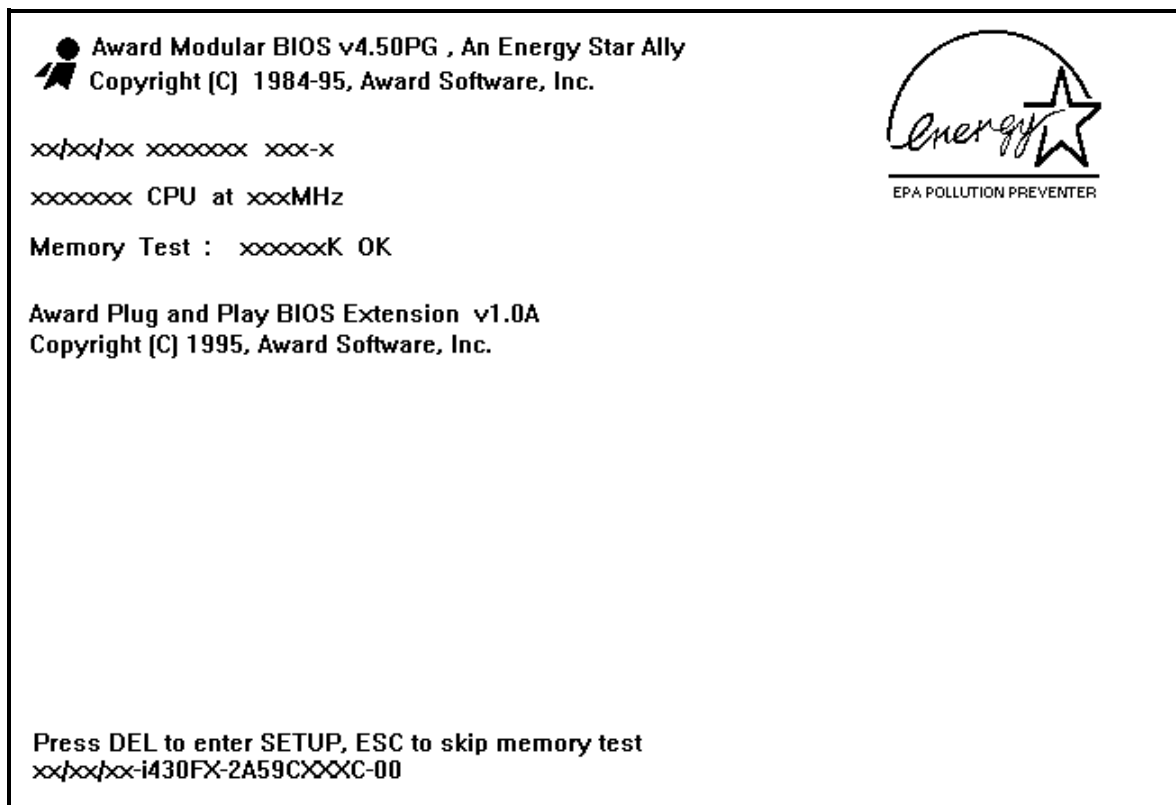


Fig. 5-1 Initial Power-On screen.

After the POST routines are completed, the following message appears :

" Press **DEL** to enter SETUP "

To execute the Award BIOS Setup program, press **DEL** key. The simulate screen in figure 5-2 MAIN MENU will be displayed at this time.

The following pages will show the simulate screens of CMOS SETUP, each figure contains the setup items and the default settings of them. Below each figure may or may not be contained a lists of function description for commonly used settings. For the other settings' function description you needed, connet to us please.

5.4 STANDARD CMOS SETUP

ROM PCI/ISA BIOS (2A59CXXX)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm : dd : yy) : Thu, Jan 11 1996																		
Time (hh : mm : ss) : 13 : 54 : 54																		
HARD DISKS	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE										
Primary Master	None	0	0	0	0	0	0	-----										
Primary Slave	None	0	0	0	0	0	0	-----										
Secondary Master	None	0	0	0	0	0	0	-----										
Secondary Slave	None	0	0	0	0	0	0	-----										
Drive A : 1.2M , 5.25 in.				<table border="1"> <tr> <td>Base Memory :</td> <td>640 K</td> </tr> <tr> <td>Extended Memory :</td> <td>xxxxxx K</td> </tr> <tr> <td>Other Memory :</td> <td>xxxxxx K</td> </tr> <tr> <td><hr/></td> <td></td> </tr> <tr> <td>Total Memory :</td> <td>xxxxxx K</td> </tr> </table>					Base Memory :	640 K	Extended Memory :	xxxxxx K	Other Memory :	xxxxxx K	<hr/>		Total Memory :	xxxxxx K
Base Memory :	640 K																	
Extended Memory :	xxxxxx K																	
Other Memory :	xxxxxx K																	
<hr/>																		
Total Memory :	xxxxxx K																	
Drive B : None																		
Video : EGA/VGA																		
Halt On : All Errors																		
ESC : Quit			↑↓→← : Select Item			PU/PD/+/- : Modify												
F1 : Help			(Shift)F2 : Change Color															

Fig. 5-3 STANDARD CMOS SETUP screen.

MODE :

For IDE hard disks, this BIOS provides three modes to support both normal size IDE hard disks and also disks size larger the 528MB:

- NORMAL : For IDE hard disks size smaller then 528MB.
- LBA : For IDE hard disks size larger then 528MB and up to 8.4GB (Giga Bytes) that use Logic Block Addressing (LBA) mode.
- Large : For IDE hard disks size larger then 528MB that do not use LBA mode. Large mode is a new specifition which may not be fully supported by all operation systems. Now it can only be used with the MS-DOS and is uncommon.

Note : Some OSes (like SCO-UNIX) must use "NORMAL" for installation.

5.5 BIOS FEATURES SETUP

ROM PCI/ISA BIOS (2A59CXXX)
 BIOS FEATURES SETUP
 AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
External Cache	: Enabled	CC000-CFFFF Shadow	: Disabled
Quick Power On Self Test	: Enabled	D0000-D3FFF Shadow	: Disabled
Boot Sequence	: A, C	D4000-D7FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	DC000-DFFFF Shadow	: Disabled
Boot Up NumLock Status	: On		
Gate A20 Option	: Fast		
Typematic Rate Setting	: Disabled		
Typematic Rate (Chars/Sec)	: 6		
Typematic Delay (Msec)	: 250		
Security Option	: Setup		
PCI/VGA Palette Snoop	: Disabled		
		ESC : Quit	↑↓→← : Select Item
		F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift)F2 : Color
		F6 : Load BIOS Default	
		F7 : Load Setup Default	

Fig. 5-4 BIOS FEATURES SETUP screen.

Virus Warning :

This feature flashes on the screen. During and after the system boots up, any attempt to write to the boot sector or partition table of the hard disk drive will halt the system and an error message will appear, in the mean time, you can run anti-virus program to locate the problem. Default values is "Disabled"

Enabled : Activate automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.

Disabled : No warning message to appear when anything attempts to access the boot sector or hard disk partition table.

CPU Internal Cache :

This option enables CPU's internal (L1) cache memory. If you want to use the internal (L1) cache memory and external (L2) cache memory, this option must be enabled.

External Cache :

This option enables L2 (secondary) external cache memory. If none external cache memory on board you must set this option to "disabled", otherwise, you can select enabled or disabled.

5.6 CHIPSET FEATURES SETUP

There are a few different setup items on this screen between 5IW and 5IS, the following three figures (Fig. 5-5, Fig. 5-6 and Fig. 5-7) show the chipset features setup screen while using either Winbond W83787F, SMC FDC37C665GT or UMC UM8669F I/O chipset.

(1) 5IW (using Winbond W83787F I/O chipset)

ROM PCI / ISA BIOS (2A59CXXX)	
CHIPSET FEATURES SETUP	
AWARD SOFTWARE, INC.	
DRAM RAS# Precharge Time : 4	PCI Concurrency : Enabled
DRAM R/W Leadoff Timing : 8/6	PCI Streaming : Enabled
DRAM RAS to CAS Delay : 3	PCI Bursting : Enabled
DRAM Read Burst Timing : x2222	Onboard FDC Controller : Enabled
DRAM Write Burst Timing : x3333	Onboard Serial Port 1 : COM1/3F8
System BIOS Cacheable : Disabled	Onboard Serial Port 2 : COM2/2F8
Video BIOS Cacheable : Enabled	Onboard Parallel Port : 378H
8 Bit I/O Recovery Time : 1	Onboard Parallel Mode : Normal
16 Bit I/O Recovery Time : 1	Serial Port 1 MIDI : Disabled
Memory Hole At 15M-16M : Disable	Serial Port 2 MIDI : Disabled
IDE HDD Block Mode : Enabled	
IDE Primary Master PIO : Auto	
IDE Primary Slave PIO : Auto	
IDE Secondary Master PIO : Auto	
IDE Secondary Slave PIO : Auto	ESC : Quit ↑↓→← : Select Item
On-Chip Primary PCI IDE : Enabled	F1 : Help PU/PD/+/- : Modify
On-Chip Secondary PCI IDE : Enabled	F5 : Old Values (Shift)F2 : Color
PCI Slot IDE 2nd Channel : Enabled	F6 : Load BIOS Default
	F7 : Load Setup Default

Fig. 5-5 CHIPSET FEATURES SETUP screen.

WARNING : *The CHIPSET FEATURES SETUP in this screen are provided so that technical professionals can modify the Chipset to suit their requirement. If you are not a technical engineer, do not use this program !*

IDE HDD Block Mode :

This feature enhances hard disk performance, making multi-sector transfers instead of one sector per transfer. Most IDE drives, except the very early designs can use this feature. Default is "Enabled".

(2) 5IS (using SMC FDC37C665GT I/O chipset)

DRAM RAS# Precharge Time : 4	PCI Concurrency : Enabled
DRAM R/W Leadoff Timing : 8/6	PCI Streaming : Enabled
DRAM RAS to CAS Delay : 3	PCI Bursting : Enabled
DRAM Read Burst Timing : x2222	Onboard FDC Controller : Enabled
DRAM Write Burst Timing : x3333	Onboard Serial Port 1 : COM1
System BIOS Cacheable : Disabled	Onboard Serial Port 2 : COM2
Video BIOS Cacheable : Enabled	Onboard Parallel Port : 378H
8 Bit I/O Recovery Time : 1	Parallel Port Mode : Normal
16 Bit I/O Recovery Time : 1	
Memory Hole At 15M-16M : Disable	
IDE HDD Block Mode : Enabled	
IDE Primary Master PIO : Auto	
IDE Primary Slave PIO : Auto	
IDE Secondary Master PIO : Auto	
IDE Secondary Slave PIO : Auto	ESC : Quit ↑↓→← : Select Item
On-Chip Primary PCI IDE : Enabled	F1 : Help PU/PD/+/- : Modify
On-Chip Secondary PCI IDE : Enabled	F5 : Old Values (Shift)F2 : Color
PCI Slot IDE 2nd Channel : Enabled	F6 : Load BIOS Default
	F7 : Load Setup Default

Fig. 5-6 CHIPSET FEATURES SETUP screen.

(3) 5IS (using UMC UM8669F I/O chipset)

DRAM RAS# Precharge Time : 4	PCI Concurrency : Enabled
DRAM R/W Leadoff Timing : 8/6	PCI Streaming : Enabled
DRAM RAS to CAS Delay : 3	PCI Bursting : Enabled
DRAM Read Burst Timing : x2222	Onboard FDC Controller : Enabled
DRAM Write Burst Timing : x3333	Onboard Serial Port 1 : COM1/3F8
System BIOS Cacheable : Disabled	Onboard Serial Port 2 : COM2/2F8
Video BIOS Cacheable : Enabled	Infra Red (IR) Function : Disabled
8 Bit I/O Recovery Time : 1	Onboard Parallel Port : 378H/IRQ7
16 Bit I/O Recovery Time : 1	Onboard Parallel Mode : SPP
Memory Hole At 15M-16M : Disable	
IDE HDD Block Mode : Enabled	IR Transfer Mode : Half-Dup
IDE Primary Master PIO : Auto	
IDE Primary Slave PIO : Auto	
IDE Secondary Master PIO : Auto	
IDE Secondary Slave PIO : Auto	ESC : Quit ↑↓→← : Select Item
On-Chip Primary PCI IDE : Enabled	F1 : Help PU/PD/+/- : Modify
On-Chip Secondary PCI IDE : Enabled	F5 : Old Values (Shift)F2 : Color
PCI Slot IDE 2nd Channel : Enabled	F6 : Load BIOS Default
	F7 : Load Setup Default

Fig. 5-7 CHIPSET FEATURES SETUP screen.

5.7 POWER MANAGEMENT SETUP

ROM PCI/ISA BIOS (2A59CXXX)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management : User Define	IRQ 3 (COM 2) : ON
PM Control by APM : No	IRQ 4 (COM 1) : ON
Video Off Method : Blank Screen	IRQ 5 (LPT 2) : OFF
	IRQ 6 (Floppy Disk) : ON
Doze Mode : 20 Min	IRQ 7 (LPT 1) : ON
Standby Mode : 20 Min	IRQ 8 (RTC Alarm) : OFF
Suspend Mode : 10 Min	IRQ 9 (IRQ2 Redir) : OFF
HDD Power Down : Disable	IRQ 10 (Reserved) : OFF
	IRQ 11 (Reserved) : OFF
IRQ3 (Wake-Up Event) : ON	IRQ 12 (PS/2 Mouse) : ON
IRQ4 (Wake-Up Event) : ON	IRQ 13 (Coprocessor) : OFF
IRQ8 (Wake-Up Event) : OFF	IRQ 14 (Hard Disk) : ON
IRQ12 (Wake-Up Event) : ON	IRQ 15 (Reserved) : OFF
Power Down Activities	
COM Ports Accessed : ON	ESC : Quit ↑↓→← : Select Item
LPT Ports Accessed : ON	F1 : Help PU/PD/+/- : Modify
Drive Ports Accessed : ON	F5 : Old Values (Shift)F2 : Color
	F6 : Load BIOS Default
	F7 : Load Setup Default

Fig. 5-8 POWER MANAGEMENT SETUP screen.

WARNING : *The POWER MANAGEMENT SETUP in this screen are provided so that technical professionals can modify the Chipset to suit their requirement. If you are not a technical engineer, do not use this program !*

Power Management :

This setting controls the Power Management functions. "User Define" allows the values of all parameters could be modified. "Min Saving", "Max Saving" or "Optimize" fixed the values of three parameters, including "Doze Mode", "Standby Mode" and "Suspend Mode". "Disable" disabled all Power Management functions. Default is "User Define".

5.8 PCI CONFIGURATION SETUP

ROM PCI / ISA BIOS (2A59CXXX)
 PCI CONFIGURATION SETUP
 AWARD SOFTWARE, INC.

PnP BIOS Auto-Config	: Enabled	
Slot 1 Using INT#	: AUTO	
Slot 2 Using INT#	: AUTO	
Slot 3 Using INT#	: AUTO	
Slot 4 Using INT#	: AUTO	
1st Available IRQ	: 9	
2nd Available IRQ	: 10	
3rd Available IRQ	: 11	
4th Available IRQ	: 12	
PCI IRQ Activated By	: Level	
PCI IDE IRQ Map To	: PCI-AUTO	
Primary IDE INT#	: A	
Secondary IDE INT#	: B	
		ESC : Quit ↑↓→← : Select Item
		F1 : Help PU/PD/+/- : Modify
		F5 : Old Values (Shift)F2 : Color
		F6 : Load BIOS Default
		F7 : Load Setup Default

Fig. 5-9 PCI CONFIGURATION SETUP screen.

WARNING : *The PCI CONFIGURATION SETUP in this screen are provided so that technical professionals can modify the PCI Configuration to suit their requirement. If you are not a technical engineer, do not use this program !*

PnP BIOS Auto-Config :

When Enabled, this parameter locks several settings (1st Available IRQ through 4th Available IRQ) and adjusts the available IRQs automatically. When Disabled, it allows the user to adjust the available IRQs individually.

Some suggestions for PCI IDE card setup :

1. PCI IDE with "Legacy Header" or simply No PCI IDE Device :
 - Choose option "ISA" in item "PCI IDE IRQ Map To".
2. Dirty PCI IDE without "Legacy Header" and without a accurate Cfg Space :
 - Check which slot is this card plug and choose PCI-SLOT1 --- PCI-SLOT4.
 - Determine the INTs for primary and secondary channel by checking the IDE cards manual or simply ask the IDE card vender or supplier.
3. Identifiable PCI IDE :
 - Choose "PCI-AUTO" for these cards.
 - Determine the INTs for primary and secondary channel by checking the IDE cards manual or simply ask the IDE card vender or supplier.

5.9 LOAD SETUP DEFAULTS

This option loads the SETUP default values from BIOS default table. By pressing "Enter" key, while "LOAD SETUP DEFAULTS" is highlighted, then presses "Y" and "Enter" key. the SETUP default values will be loaded. The SETUP default settings are the best-case values that should optimize system performance. If CMOS RAM is corrupted, the SETUP DEFAULTS settings are loaded automatically.

5.10 PASSWORD SETTING

Type the Password and press "Enter" repeat. Enters up to eight alphanumeric characters. By pressing "Enter" key twice, without any alphanumeric character enters, the PASSWORD will be disabled.

5.11 IDE HDD AUTO DETECTION

By pressing "Enter" key, while "IDE HDD AUTO DETECTION" is highlighted causes the system to attempt to detect the type of hard disk. If successful, then presses "Y" (or 1, 2, ...) and "Enter" key, it fills in the remaining fields on this menu and the correlated fields in the STANDARD CMOS SETUP menu.

5.12 SAVE & EXIT SETUP

This option saves all setup values to CMOS RAM & EXIT SETUP routine, by moving the cursor to "SAVE & EXIT SETUP" and pressing "Enter" key, then types "Y" and "Enter" key, the values will be saved, the setup program will be terminated and the system will be reboot.

5.13 EXIT WITHOUT SAVING

This option exits setup routine without saves any changed values to CMOS RAM, by moving the cursor to "EXIT WITHOUT SAVING" and pressing "Enter" key, then types "Y" and "Enter" key, the setup program will be terminated and the system will be reboot.