

PT-5VMX

VIA MVP3

ATX MAINBOARD

OPERATION MANUAL

VIA MVP3 ATX SYSTEM BOARD

OPERATION MANUAL

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TRADEMARKS

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NOTE

The “LOAD SETUP DEFAULTS” function loads the default settings directly from BIOS default table, these default settings are the best-case values that will optimize the system performance and increase the system stability. This is strongly recommended when you first receive this system board, or the system CMOS data is corrupted.

Move the selection bar to “LOAD SETUP DEFAULTS” and then press the “ENTER” key and then the SETUP default values will be loaded into the system. (Please refer to the Chapter 4 AWARD BIOS SETUP procedures in this manual.)

NOTICE

Information presented in this manual has been carefully checked for reliability; however, no responsibility is assumed for inaccuracies. The information contained in this manual is subject to change without prior notice.

1. INTRODUCTION

1.1 SYSTEM OVERVIEW

This mainboard is an ATX form-factor PCI Local Bus Pentium™ system board with the updated AGP interface designed onboard. The most updated VIA MVP3 chipset for 100MHz Front Side Bus (FSB) is chosen for this mainboard and it gives the most outstanding performance for different applications.

This mainboard is designed for the high performance Pentium™ or other equivalent processors for high-end application and it is a true GREEN-PC computer system. The FSB (Front Side Bus) clock speed can be adjusted to 100MHz when we are installing the 100MHz FSB processor.

This system board supports the Peripheral Component Interconnect (PCI) Local Bus standard (PCI Specification Rev. 2.1 compliant). It not only breaks through the I/O bottlenecks of the traditional ISA mainboard, but also provides the ultra high performance for networking and multi-user environments.

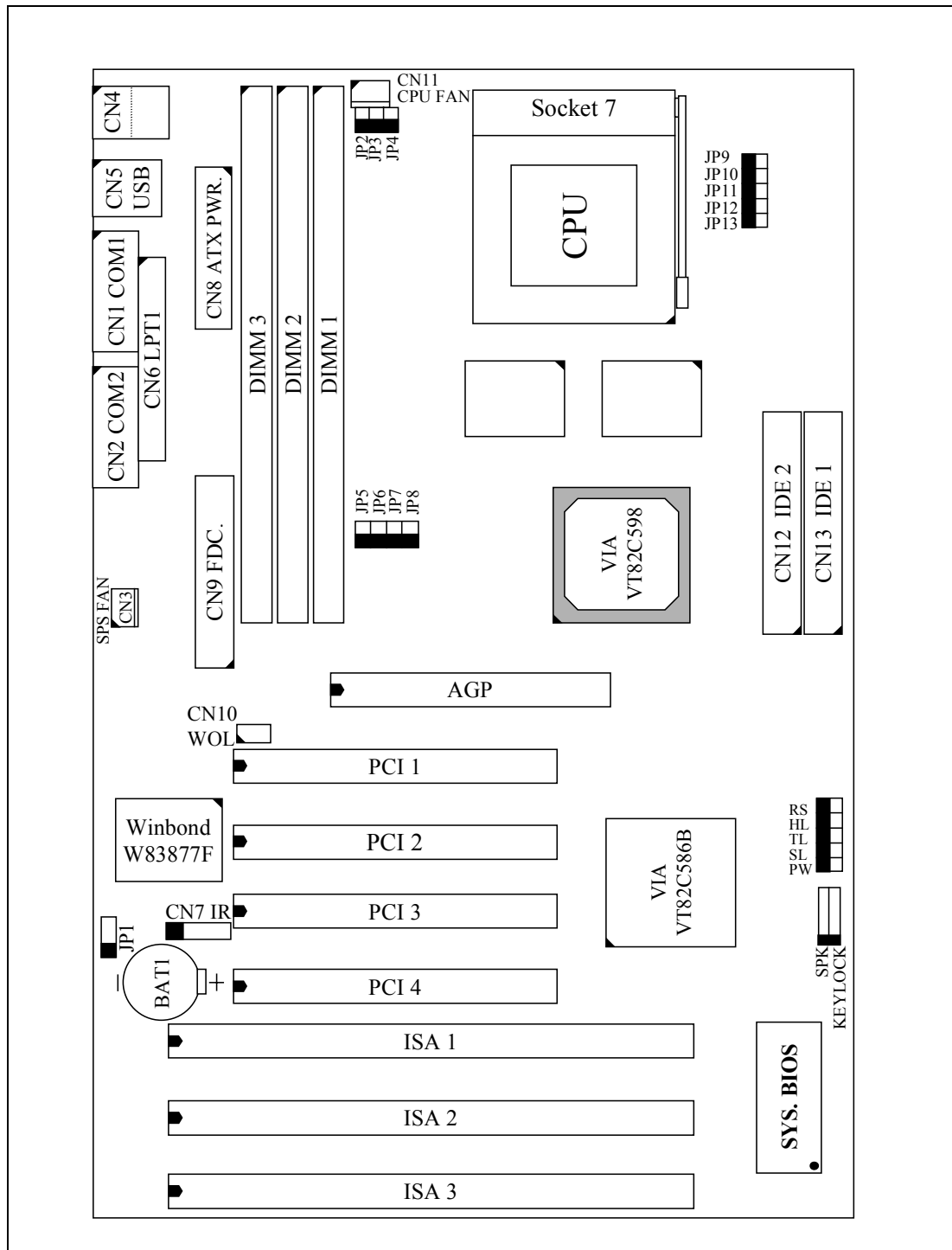
The mainboard has built-in two channels PIO and Bus Master Enhanced PCI IDE port, one Floppy Disk control port, two high speed Serial ports (UARTs), one multi-mode Parallel port, one PS/2 keyboard port, one PS/2 mouse port, one IR port, two USB ports.

The Accelerated Graphic Port (A.G.P.) on the board is designed for the updated AGP 3D video display card. Unlike the traditional PCI-based display cards, AGP technology provides lightening data throughput to fully facilitate the 3Dimensional and multimedia graphic display. The data transfer rate on the AGP port can be as fast as 133MHz and it is much faster than the traditional 33MHz PCI VGA cards.

The AGP is a new video display technology and it requires the device driver or new operating system to enable the accelerated graphic feature. Windows® 98 will support AGP directly, but Windows® 95 still needs the appropriate device drivers to enable the AGP feature. Please don't worry about the device driver, you can always find the device driver included in the AGP card.

1.2 SYSTEM BOARD LAYOUT

Explanation : The connectors, jumpers and components which has the black point marked on the corner means the location of pin-1 side of the connector, jumper and component.



2. FEATURES

2.1 MAINBOARD SPECIFICATIONS

❑ Chipset

VIA MVP3 (VT82C598MVP, VT82C586B) and Winbond W83877F / TF.

❑ CPU

Intel : Pentium™ processor and OverDrive processor

90 / 100 / 120 / 133 / 150 / 166 / 200 / 233 MHz.

Cyrix : 6x86 / 6x86L - P150+ / P166+ / P200+.

6x86MX - PR166 / PR200 / PR233, 6x86MII - 266/300/333/366

IBM : 6x86MX - PR166 / PR200 / PR233 / PR266/PR300/PR333

AMD : K5 - PR90 / PR100 / PR120 / PR133 / PR150 / PR166.

K6-166 / 200 / 233 / 266 / 300

K6-2 -300 / 333 / 350 / 366 / 380 / 400 / 450.

K6-3 -400 / 450.

IDT : Win Chip C6-180 / 200 / 225 / 240.

WinChip 2A - 200 / 233 / 266 / 300.

WinChip 3 - 266 / 300 / 333 / 350.

❑ CPU Voltage

(1).CPU I/O voltage : “+3.3V DC” or “+3.5V DC”.

(2).CPU CORE voltage: +1.3V DC ~ +3.5V DC.

❑ System Clock

60 / 66 / 75 / 83 / 95 / 100 MHz

❑ Memory

DRAM : Three banks, each bank can be single or double sided. Memory size up to 1GB. Supports SDRAM memory (use 168 pin DIMM module x 3).

Supports Parity / ECC (Error Checking and Correcting)

SRAM : 512KB or 1MB (optional) pipelined burst SRAM on board.

❑ BIOS

AWARD System BIOS. 128KB x 8 Flash ROM (for Plug & Play BIOS).

Expansion Slots

AGP Slots: 32-bit x 1 (Supports 1x/2x AGP graphics cards)

PCI Slots : 32-bit x 4 (All Master / Slave, PCI 2.1 Compliant).

ISA Slots : 16-bit x 3 (PCI / ISA slot share one slot).

☐ **IDE Ports**

Two channel PIO and “Ultra DMA/33” Bus Master PCI IDE ports, which will connect maximum 4 IDE devices like IDE Hard Disk and ATAPI CD-ROM device. PIO Mode 4 transfer rate up to 14 Mbytes/s transfer rates and supports “Ultra DMA/33” mode transfers up to 33 Mbytes/sec.

☐ **ACPI**

- 1.Power on by Panel-Switch, or Modem Ring-in or LAN signal.
- 2.Power off (Soft-off) by OS or Panel-Switch.
- 3.Resume by several system devices (such as modem ring-in, RTC alarm).

☐ **WOL**

One WOL connector supports Wake-On-LAN.

☐ **USB Ports**

Two Universal Serial Bus (USB) ports.

☐ **Super I/O Ports**

- 1.Two high speed NS16C550 compatible Serial ports (UARTs).
- 2.One SPP / EPP / ECP mode Bi-directional parallel port.
- 3.One Floppy Disk Control port.

☐ **IR Port**

One HPSIR and ASKIR compatible Infrared port.

☐ **Mouse and Keyboard**

Supports PS/2 Mouse connector, PS/2 Keyboard connector

☐ **Software compatibility**

MS-DOS, Windows NT, OS/2, UNIX, NOVELL, MS Windows, CAD/CAM, Windows 98 (Beta), ...etc.

❑ DIMENSION

Width & Length : 304 mm x 200 mm.

Height : 3/4 inches with components mounted.

PCB Thickness : 4-layers, 0.05 inches normal.

Weight : 20 ounces.

❑ ENVIRONMENT

Operating Temperature : 10°C to 40°C. (50°F to 104°F).

Require Airflow : 50 linear feet per minute across CPU.

Storage Temperature : -40°C to 70°C. (-40°F to 158°F).

Humidity : 0 to 90% non-condensing.

Altitude : 0 to 10,000 feet.

2.2 AMAZING WAYS TO POWER ON THE PC SYSTEM

When the mainboard has been installed successfully, there are several ways to power on the system. Please read the following description for all the details.

❑ POWER BUTTON

The power button can be programmed by COMS setup program and it has different features. Please refer to page 3-11 for detail function description.

❑ RTC ALARM

PC system can be waked up by the RTC setting in the CMOS. You can set the alarming date and time in the RTC memory, When RTC alarms, the PC system will be triggered and wakes up automatically.

Enable the “Resume by Alarm” selection in the BIOS setup utility, and then input the accurate date and time in following fields. (the “Resume by Alarm” is located in the “POWER MANAGEMENT SETUP”, please refer to Section 4-7), Having stored the RTC alarm setting, the PC system will be turned on automatically according to the date and time which is recorded in the CMOS memory.

Same as the above, you have to reboot the PC system and wait for the POST (Power On Self Test) is completed to enable the RTC alarm.

□ MODEM RING-IN

Everyone knows that a PC system can be used as a fax machine to send or receive fax messages. But most people still use fax machine to receive their messages because it is not practical to have the system powered on all day long waiting for the incoming messages. Now the problem can be solved by using this mainboard. This mainboard can be triggered by a modem ring-in signal. When you have a **external** modem installed, you can leave the PC system power off. Whenever there is the incoming message, the PC system will be triggered by the ring-in signal and wake up automatically to receive the message for you. From now on, you can tell your PC system to receive the fax message for you.

In order to use the ring-in signal to wake up your PC system, you will have to use the **EXTERNAL MODEM** and have it connected to one of the **SERIAL PORTS** (COMA or COM B). When the system power is off, this mainboard will continue to detect the serial port status. When it detects the ring-in signal from the serial port, the system power will be turned on and start to receive the incoming messages automatically.

To enable the Modem Ring-In feature, you have to run the BIOS setup utility and enable the “Resume by Ring or LAN” option (it is located in the “POWER MANAGEMENT SETUP”, please refer to Section 4-7 for the settings). Having completed the BIOS setup, you have to reboot the PC system so that BIOS can verify the setting. (the “DMI pool data” will be verified by the BIOS when loading the operating system). Simply speaking, shut down the PC system and then re-start the system. The modem ring-in feature will be enabled when the operation system has been loaded.

Note: This function is not available when using the internal MODEM card.

□ WAKE ON LAN (WOL)

There is a WOL connector CN10 (see page 3-8) on the mainboard which is designed to connect to the signal from a LAN card which supports the Wake On LAN feature. When such LAN card is installed, you may turn on the PC system from your remote server and monitor the PC status.

To enable this feature, you will have to use the BIOS setup utility to enable the “Resume by Ring or LAN” (it is located at “POWER MANAGEMENT SETUP”, please refer to Section 4-7 for the settings). Having completed the BIOS setup, you have to reboot the PC system so that BIOS can verify the setting. (the “DMI pool data” will be verified by the BIOS when loading the operating system). Simply speaking, reboot the PC system, the Wake On LAN feature will be enabled when the operation system has been loaded

***Note:** This function will be disabled if you turn off the power before the system can verify the DMI pool data.*

2.3 POWER OFF THE PC SYSTEM

There are two ways to power off the system. They are “Shut Down by Power Button” and “ Shut Down by OS”. (such as Windows® 95 and Windows® 98, you can choose the **Shut Down** from the file menu and the system will be powered off immediately).

3. HARDWARE SETUP

This chapter explains how to configure the mainboard hardware. When you are installing the mainboard, you will have to make jumper settings and cable connections. Please refer to the following sections for the details:

3.1 UNPACKING

The system board package contains the following parts :

- This system board.
- Operation manual.
- A CD diskette which includes device driver and utility program

The mainboard contains electric sensitive components which can be easily damaged by static electricity, please leave the mainboard sealed in its original packing until when installation.

Unpacking and installation shall be done on a grounded anti-static mat. The operator will have to wear an anti static wristband, grounded at the same point as the anti-static mat.

Inspect the mainboard carton to see whether there is any obvious damage. Shipping and handling may cause damage to your board. Be sure there is no shipping or handling damages on the board before proceeding.

After opening the motherboard color box, extract the mainboard and place it only on a grounded anti-static surface with the component side up. Inspect the board again to see whether there is any damage.

Press on all sockets of IC's to make sure that they are properly seated. Please put the mainboard on a firm flat surface when you are installing the component to the socket on the mainboard..

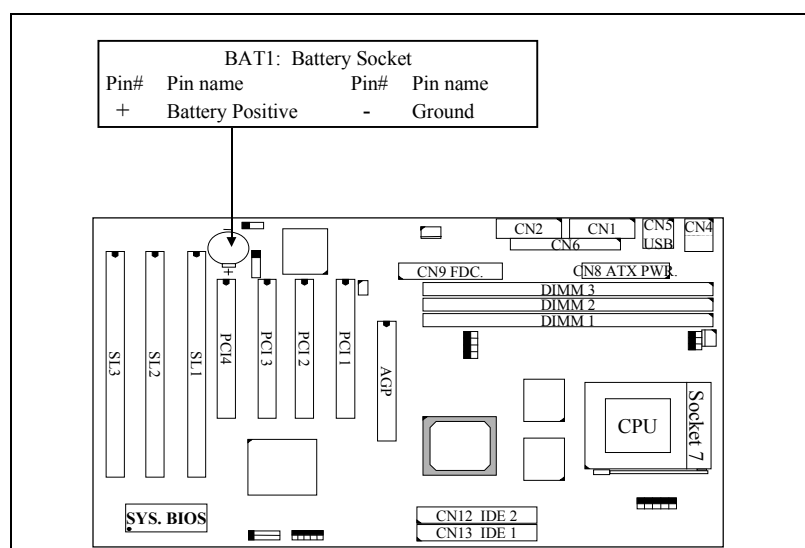
3.2 HARDWARE CONFIGURATION

Before the system board is ready for operating, the hardware must be configured to make sure it will work properly with different environment. To configure the system board is a simple task, only a few jumpers, connectors, cables and sockets needs to be selected and installed.

3.2.1 CONNECTORS

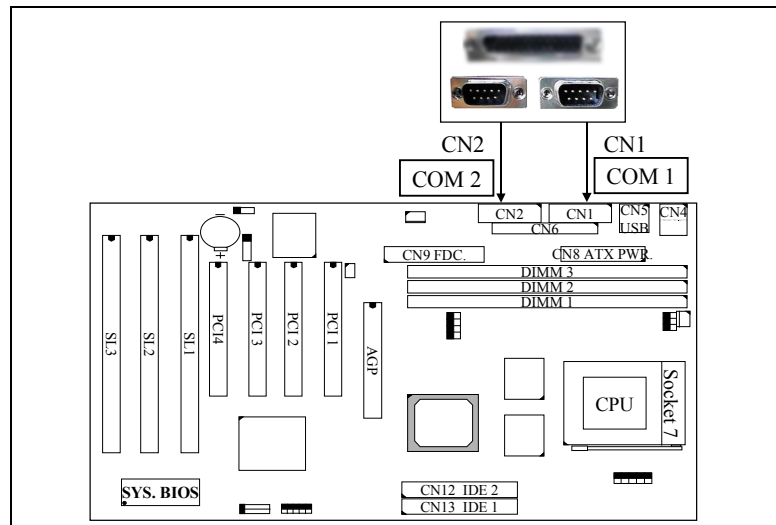
A connector is two or more pins that are used make connections to the system standard accessories (such as power, mouse, printer,...etc.). The following is a list of connectors on board, as well as descriptions of each individual connector.

(A) BAT1 Non-rechargeable battery (Use 3V Lithium battery : CR2032)



(B) CN1 COM 1 (Serial Port 1) connector

(C) CN2 COM 2 (Serial Port 2) connector

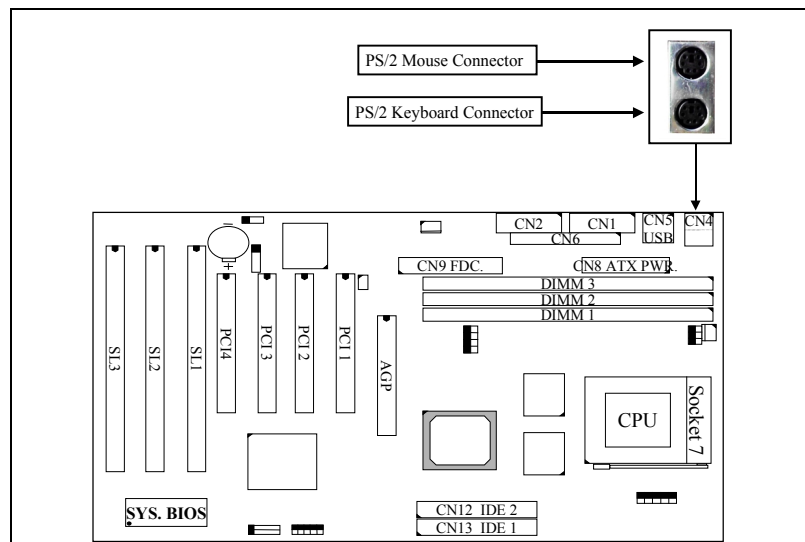


Ping assignment of serial port connector:

1	6	Pin #	Signal name	Pin #	Signal name
<input type="checkbox"/>	<input type="checkbox"/>	1	DCD (Data Carrier Detect)	6	DSR (Data Set Ready)
<input type="checkbox"/>	<input type="checkbox"/>	2	RD (Received Data)	7	RTS (Request To Send)
<input type="checkbox"/>	<input type="checkbox"/>	3	TD (Transmit Data)	8	CTS (Clear To Send)
<input type="checkbox"/>	<input type="checkbox"/>	4	DTR (Data Terminal Ready)	9	RI (Ring Indicator)
<input type="checkbox"/>		5	Ground		
5	9				

I/O address 3F8H/2F8H/3E8H/2E8H, IRQ3/IRQ4, selected by CMOS setup.

(D) CN4 PS/2 Mouse and Keyboard Connector

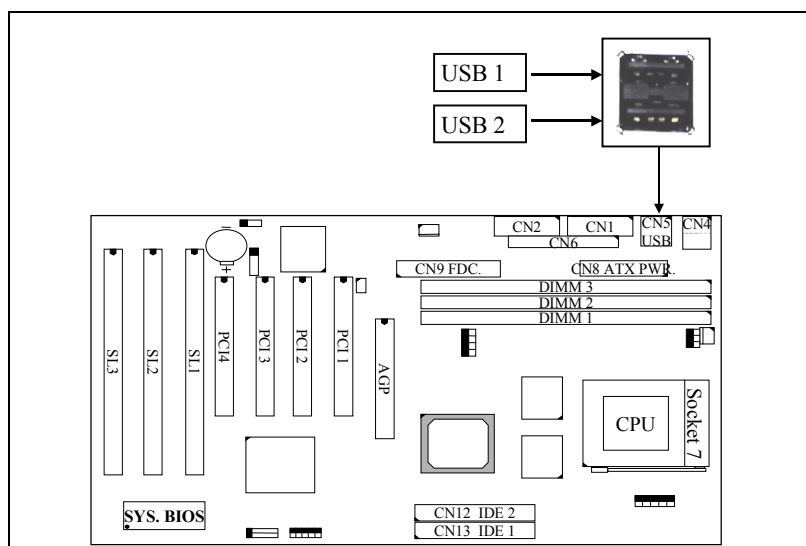
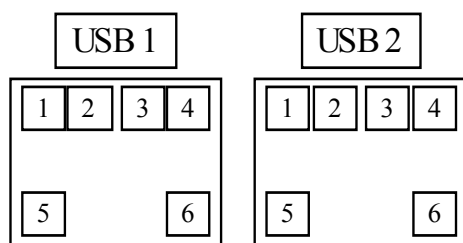


Pin assignment of PS/2 mouse connector:

<u>Pin #</u>	<u>Signal name</u>	<u>Pin #</u>	<u>Signal name</u>	<u>Pin #</u>	<u>Signal name</u>
1	Mouse Data	3	Ground	5	Mouse Clock
2	No Connection	4	+ 5V DC	6	No Connection

Pin assignment of keyboard connector

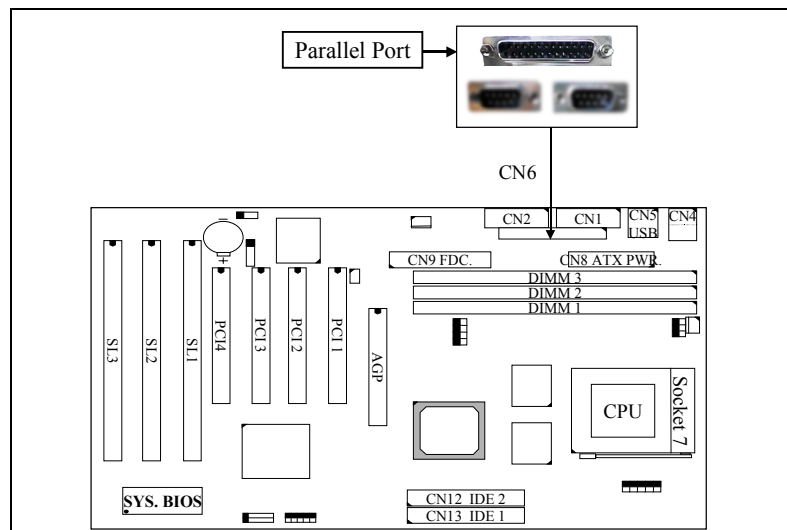
<u>Pin #</u>	<u>Signal name</u>	<u>Pin #</u>	<u>Signal name</u>	<u>Pin #</u>	<u>Signal name</u>
1	Keyboard Data	3	Ground	5	Keyboard Clock
2	No Connection	4	+ 5V DC	6	No Connection

(E) CN5 USB (Universal Serial Bus) connector**Pin assignment of USB connector:**

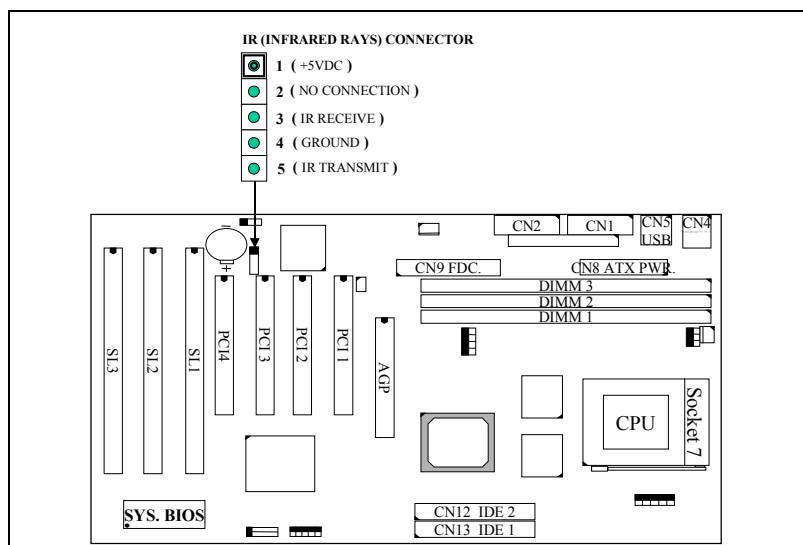
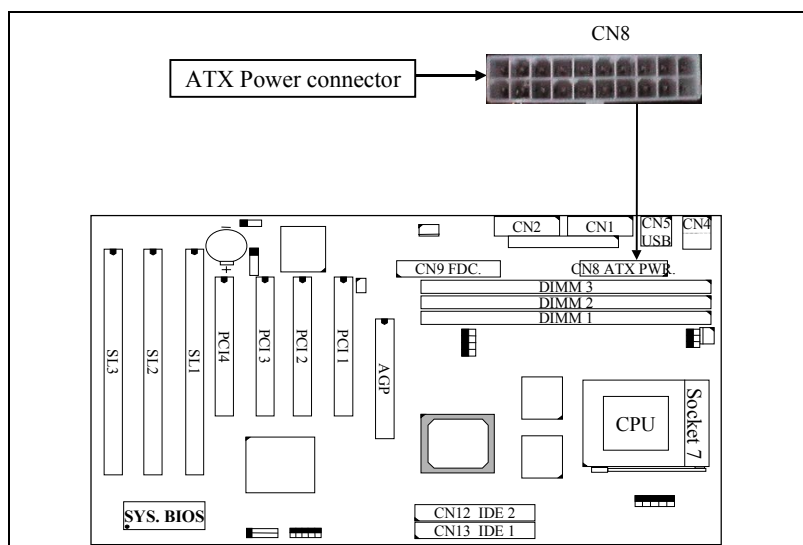
Pin1: +5VDC
 Pin2: DATA-
 Pin3: DATA+
 Pin4: Ground
 Pin5: Ground
 Pin6: Ground

(F) CN6 Parallel Port Connector

(Supports SPP/EPP/ECP mode, using IRQ7 or IRQ5, ECP modes use DMA channel 3 or channel 1, and it can be programmed by CMOS setup)

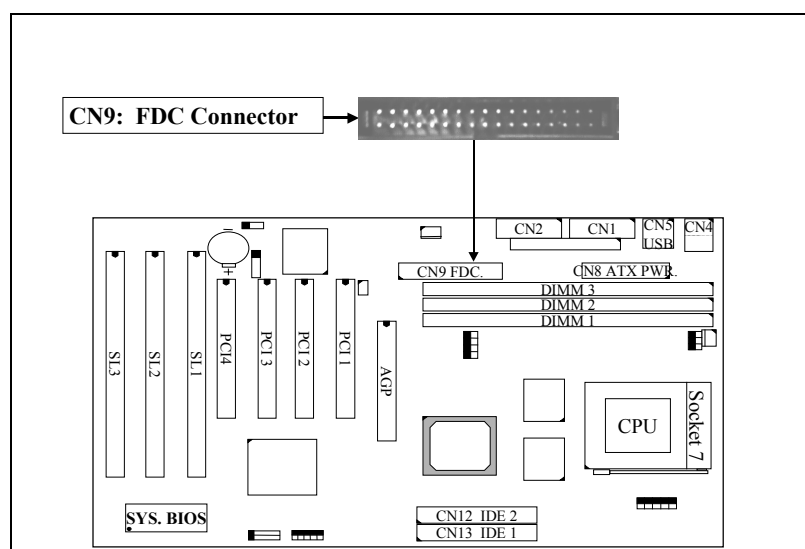
**Pin assignment of parallel port:**

1	14	Pin #	Signal name	Pin #	Signal name
<input type="checkbox"/>	<input type="checkbox"/>	1	STROBE <input type="checkbox"/>	14	AUTO FEED <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	2	Data Bit 0	15	ERROR <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	3	Data Bit 1	16	INIT <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	4	Data Bit 2	17	SLCT IN <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	5	Data Bit 3	18	Ground
<input type="checkbox"/>	<input type="checkbox"/>	6	Data Bit 4	19	Ground
<input type="checkbox"/>	<input type="checkbox"/>	7	Data Bit 5	20	Ground
<input type="checkbox"/>	<input type="checkbox"/>	8	Data Bit 6	21	Ground
<input type="checkbox"/>	<input type="checkbox"/>	9	Data Bit 7	22	Ground
<input type="checkbox"/>	<input type="checkbox"/>	10	ACK <input type="checkbox"/>	23	Ground
<input type="checkbox"/>	<input type="checkbox"/>	11	BUSY	24	Ground
<input type="checkbox"/>	<input type="checkbox"/>	12	PE	25	Ground
<input type="checkbox"/>		13	SLCT		
13	25				

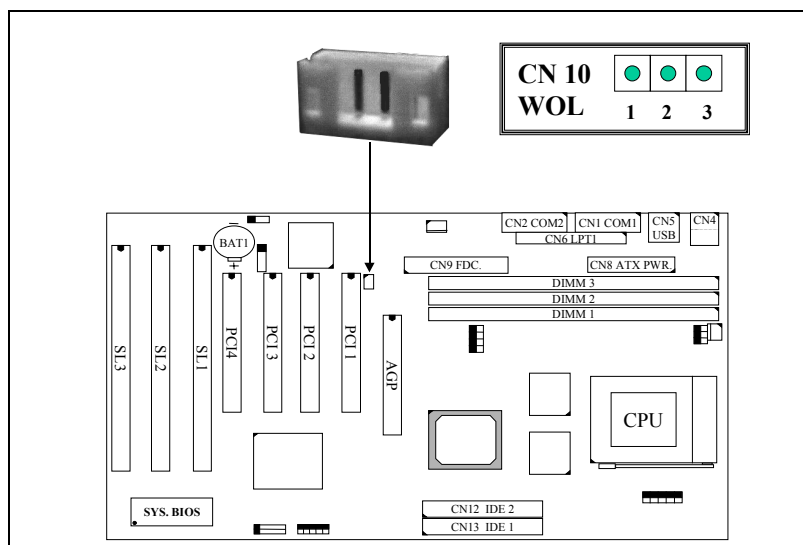
(G) CN7 IR (Infrared Rays) transmission connector**(H) CN8 ATX Power connector**

Pin assignment of ATX power connector

11	1	Pin #	Signal name	Pin #	Signal name
<input type="checkbox"/>	<input type="checkbox"/>	11	+ 3.3V DC	1	+ 3.3V DC
<input type="checkbox"/>	<input type="checkbox"/>	12	- 12V DC	2	+ 3.3V DC
<input type="checkbox"/>	<input type="checkbox"/>	13	Ground	3	Ground
<input type="checkbox"/>	<input type="checkbox"/>	14	PS-ON	4	+ 5V DC
<input type="checkbox"/>	<input type="checkbox"/>	15	Ground	5	Ground
<input type="checkbox"/>	<input type="checkbox"/>	16	Ground	6	+ 5V DC
<input type="checkbox"/>	<input type="checkbox"/>	17	Ground	7	Ground
<input type="checkbox"/>	<input type="checkbox"/>	18	- 5V DC	8	PW-OK
<input type="checkbox"/>	<input type="checkbox"/>	19	+ 5V DC	9	+ 5V SB
<input type="checkbox"/>	<input type="checkbox"/>	20	+ 5V DC	10	+ 12V DC
20	10				

(I) CN9 Floppy Disk Control Port connector (Using IRQ6, DMA channel 2)**(J) CN10: WOL (Wake On LAN) Connector**

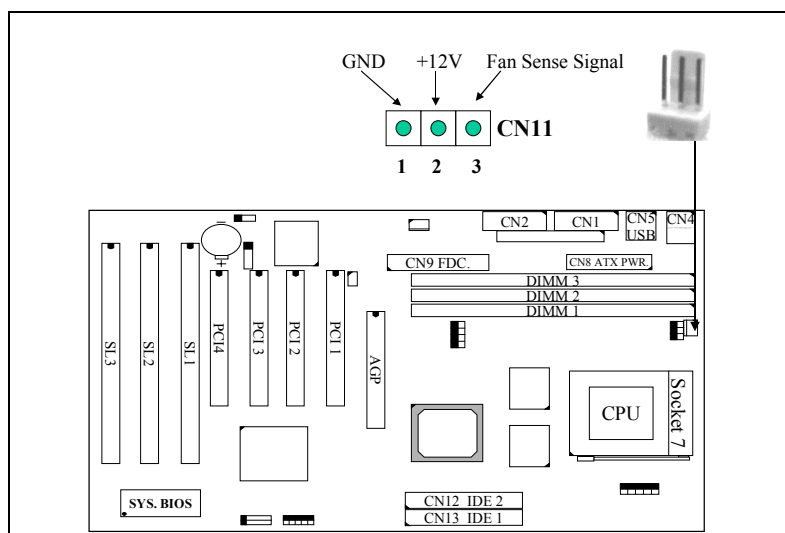
In order to use the WOL LAN card to trigger the power of the PC system, the switching power supply must be able to provide at least 700mA current driving ability on the “5V standby” voltage.



Pin assignment of WOL Connector

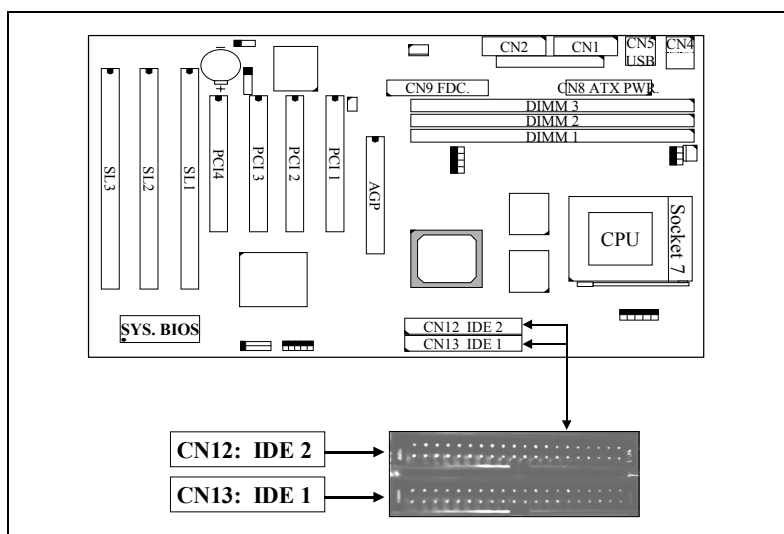
1	2	3	Pin #	Signal name	Pin #	Signal name	Pin #	Signal name
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	1	5V standby	2	Ground	3	WOL Signal

(K) CN11 CPU Cooling Fan Power connector (*optional*)

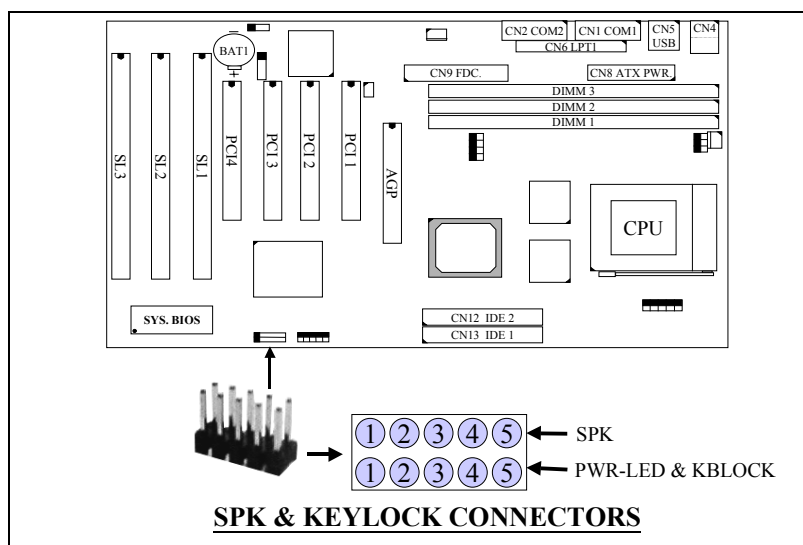


(L) CN12 IDE 1 Connector (Primary IDE Port, using IRQ14)

(M) CN13 IDE 2 Connector (Secondary IDE Port, using IRQ15)



(N) SPK & KEYLOCK Connector:



1. SPK: Speaker connector

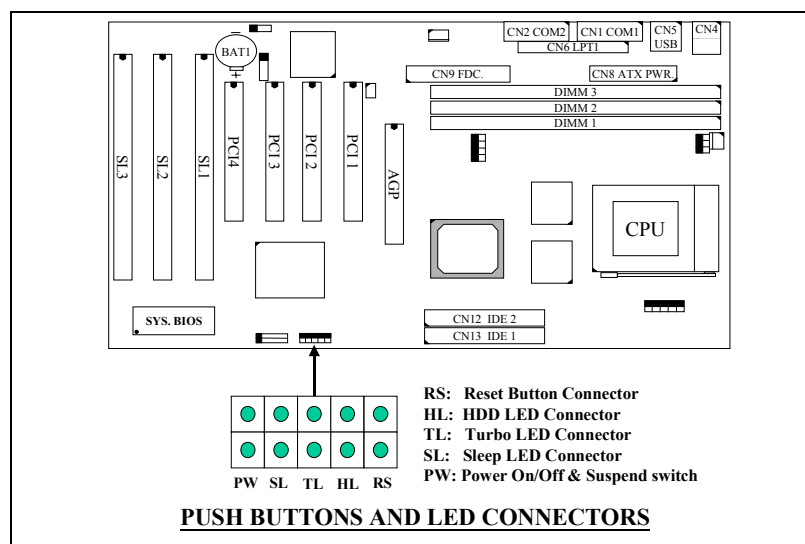
1	Pin #	Assignment
●	1	+5V DC
●	2	No Connection
●	3	No Connection
●	4	Speaker Data Signal

2. KEYLOCK Connector: Front Panel Power LED & Key-Lock connector

1	Pin #	Assignment
●	1	Pullup (+5V DC for Power LED)
●	2	No Connection
●	3	Ground
●	4	Keyboard Lock
●	5	Ground
5		

(O) Push buttons and LED connectors

A series of connectors are designed on the board to connect the push buttons and LED indicators. Please see the following for the details:



1. RS: Reset Button connector

Open : No action

Short : System Reset

Pin # Assignment

Pin # Assignment

1 Reset Control

2 Ground

2. HL: IDE HDD LED connector

Pin # Assignment

Pin # Assignment

1 Pullup (+5V DC)

2 Signal Pin

3. TL: Turbo LED connector

Pin # Assignment

1 Pullup (+5V DC)

2 Ground

4. SL: Sleep LED Connector

This LED will be lightened when the AC power is connected and the system is power off, darkened when the AC power is disconnected or the system is powered on.

<u>Pin #</u>	<u>Signal name</u>
1	Signal Pin
2	Ground

5. PW: Power On/Off and External Suspend Switch Connector

According to the setup in CMOS, the PW connector has two functions. It can be the Power Switch or Suspend Switch of your PC system. (please refer to Section- 4-7 “Soft-Off by PWRBTN”)

(1) The setup in CMOS is “Instant-off”:**A. When system power is off :**

Click on this switch, the system will be powered on immediately.

B. When system power is on :

Click on this switch, the system will be powered off instantly

(2) If the setup in CMOS is “Delay 4 Sec.”, the switch function will be:**A. When system is power off :**

Press this switch, the system will power on immediately.

B. When system power is on :**a. The system is in Full-ON mode :**

a-1. Click on this switch (less than 4 seconds), the system will be turned into Suspend mode. (get into a GREEN mode)

a-2. Press and hold this switch for more than 4 seconds, the system will be powered off.

b. When the system is in Suspend mode :

b-1. Click on this switch (less than 4 seconds), the system will return to Full-ON mode.

b-2. Press and hold this switch more than 4 seconds, the system will be powered off.

3.2.2 JUMPERS

A jumper is a set of two, three or more jumper pins which allows you to make different system configuration by putting the plastic connector plug (mini-jumper) on it. The jumper setting is necessary when installing different components onto the mainboard. ***Please make sure all jumper settings are correct before you can installation the mainboard into the PC system.***

(A) JP1 Clear CMOS button

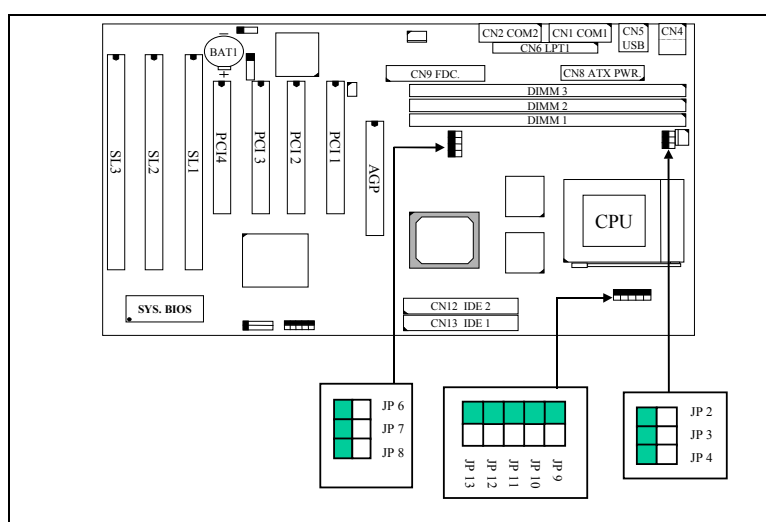
<u>Pin #</u>	<u>Function</u>
1 - 2	Normal Operation
2 - 3	Clear CMOS

Note: Improper BIOS setting may cause hang-up to the PC system, In case that it be happened and you can not handle your PC system any more, you can use JP1 to clear the system configuration information which is stored in the CMOS memory and get the PC system back to normal status.. Due to the VIA MVP3 chipset features, Clear the CMOS when the power is on is recommended. Please refer to the following steps to clear the CMOS

- 1. Open the system cabinet and leave the system power on.***
- 2. Move the mini-mumper to Pin2 and Pin3.***
- 3. Click on the Reset button to reboot the PC system to clear the CMOS.***
- 4. Return the mini-jumper to its normal position (Pin1 and Pin2).***

(B) JP2~ JP4, JP6~JP8: CPU frequency selection

(C) JP9~JP13: CPU Voltage selection



MVP3 ATX SYSTEM BOARD
AWARD BIOS SETUP

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	60MHz x 1.5	V _{CORE} = 3.5V		66MHz x 1.5	V _{CORE} = 3.5V
AMD K5-PR90 K5-PR120	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	AMD K5-PR100 K5-PR133	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	60MHz x 2.5	V _{CORE} = 3.5V		66MHz x 2.5	V _{CORE} = 3.5V
AMD K5-PR150	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	AMD K5-PR166	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	66MHz x 2.5	V _{CORE} = 2.9V		66MHz x 3	V _{CORE} = 2.9V
AMD K6 / PR2 -166	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	AMD K6 / PR2 -200	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
AMD K6 - 233	66MHz x 3.5	V _{CORE} = 3.2V	AMD K6 - 266 K6-2/266	66MHz x 4	V _{CORE} = 2.2V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
AMD K6 - 300	66MHz x 4.5	V _{CORE} = 2.2V	AMD K6-2/300	100MHz x 3	V _{CORE} = 2.2V
	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
AMD K6-2/333	95MHz x 3.5	V _{CORE} = 2.2V	AMD K6-2/350	100MHz x 3.5	V _{CORE} = 2.2V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
AMD K6-2/366	66MHz x 5.5	V _{CORE} = 2.2V	AMD K6-2/380	95MHz x 4	V _{CORE} = 2.2V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
AMD K6-2/400	100MHz x 4	V _{CORE} = 2.2V	AMD K6-2/450	100MHz x 4.5	V _{CORE} = 2.4V
	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
AMD K6-3/400	100MHz x 4	V _{CORE} = 2.4V	AMD K6-3/450	100MHz x 4.5	V _{CORE} = 2.4V
	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	66MHz x 2	V _{CORE} = 3.5V		66MHz x 2	V _{CORE} = 2.8V
Cyrix / IBM 6x86 -P166+	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	Cyrix / IBM 6x86L -P166+	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>























CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	75MHz x 2	V _{CORE} = 3.5V		75MHz x 2	V _{CORE} = 2.8V
Cyrix / IBM 6x86 -P200+	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	Cyrix / IBM 6x86L -P200+	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>























CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	66MHz x 2	V _{CORE} = 2.9V		66MHz x 2.5	V _{CORE} = 2.9V
Cyrix / IBM 6x86MX -PR166	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	Cyrix / IBM 6x86MX -PR200 (66MHz Bus)	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>























CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	75MHz x 2	V _{CORE} = 2.9V		66MHz x 3	V _{CORE} = 2.9V
Cyrix / IBM 6x86MX -PR200 (75MHz Bus)	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	Cyrix / IBM 6x86MX -PR233 (66MHz Bus)	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	75MHz x 2.5	V _{CORE} = 2.9V		83MHz x 2.5	V _{CORE} = 2.9V
Cyrix / IBM 6x86MX -PR233 (75MHz Bus)	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	Cyrix 6x86MII -266 / IBM 6x86MX -PR266	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
	66MHz x 3.5	V _{CORE} = 2.9V		75MHz x 3	V _{CORE} = 2.9V
Cyrix 6x86MII -300 / IBM 6x86MX -PR300 (66MHz Bus)	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>	Cyrix 6x86MII -300 / IBM 6x86MX -PR300 (75MHz Bus)	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
Cyrrix 6x86MII -333 / IBM 6x86MX -PR333	83MHz x 3	V _{CORE} = 2.9V	Cyrrix 6x86MII -366	100MHz x 2.5	V _{CORE} = 2.9V
	1 2	1 2		1 2	1 2
	 JP2	 JP9		 JP2	 JP9
	 JP3	 JP10		 JP3	 JP10
	 JP4	 JP11		 JP4	 JP11
	 JP6	 JP12		 JP6	 JP12
	 JP7	 JP13		 JP7	 JP13
	 JP8			 JP8	

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
IDT C6-180	60MHz x 3	V _{CORE} = 3.5V	IDT C6-200	66MHz x 3	V _{CORE} = 3.5V
	1 2	1 2		1 2	1 2
	 JP2	 JP9		 JP2	 JP9
	 JP3	 JP10		 JP3	 JP10
	 JP4	 JP11		 JP4	 JP11
	 JP6	 JP12		 JP6	 JP12
	 JP7	 JP13		 JP7	 JP13
	 JP8			 JP8	

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
IDT C6-225	75MHz x 3	V _{CORE} = 3.5V	IDT C6-240	60MHz x 4	V _{CORE} = 3.5V
	1 2	1 2		1 2	1 2
	 JP2	 JP9		 JP2	 JP9
	 JP3	 JP10		 JP3	 JP10
	 JP4	 JP11		 JP4	 JP11
	 JP6	 JP12		 JP6	 JP12
	 JP7	 JP13		 JP7	 JP13
	 JP8			 JP8	

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
IDT WinChip2A 200	66MHz x 3	V _{CORE} = 3.5V	IDT WinChip2A 233	66MHz x 3.5	V _{CORE} = 3.5V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>		<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>























CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
IDT WinChip2A 266	100MHz x 2.33	V _{CORE} = 3.5V	IDT WinChip2A 300	100MHz x 2.5	V _{CORE} = 3.5V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>























CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
IDT WinChip 3 266	66MHz x 3.5	V _{CORE} = 2.8V	IDT WinChip3 300	66MHz x 4	V _{CORE} = 2.8V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>












CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
IDT WinChip3 333	100MHz x 2.66	V _{CORE} = 2.8V	IDT WinChip3 350	95MHz x 3	V _{CORE} = 2.8V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>		<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input type="checkbox"/> <input type="checkbox"/> JP7</div> <div><input type="checkbox"/> <input type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
Intel 80502-90	60MHz x 1.5	V _{CORE} = 3.3V	Intel 80502-100	66MHz x 1.5	V _{CORE} = 3.3V
	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>		<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
Intel 80502-120	60MHz x 2	V _{CORE} = 3.3V	Intel 80502-133	66MHz x 2	V _{CORE} = 3.3V
	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>		<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP3</div> <div><input type="checkbox"/> <input type="checkbox"/> JP4</div> <div><input type="checkbox"/> <input type="checkbox"/> JP6</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8</div>	<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
Intel 80502-166	66MHz x 2.5	V _{CORE} = 3.3V	Intel 80502-200	66MHz x 3	V _{CORE} = 3.3V
	<div>1 2</div> <div> JP2</div> <div> JP3</div> <div> JP4</div> <div> JP6</div> <div> JP7</div> <div> JP8</div>	<div>1 2</div> <div> JP9</div> <div> JP10</div> <div> JP11</div> <div> JP12</div> <div> JP13</div>		<div>1 2</div> <div> JP2</div> <div> JP3</div> <div> JP4</div> <div> JP6</div> <div> JP7</div> <div> JP8</div>	<div>1 2</div> <div> JP9</div> <div> JP10</div> <div> JP11</div> <div> JP12</div> <div> JP13</div>

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13	CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
Intel 80503-166	66MHz x 2.5	V _{CORE} = 2.8V	Intel 80503-200	66MHz x 3	V _{CORE} = 2.8V
	<div>1 2</div> <div> JP2</div> <div> JP3</div> <div> JP4</div> <div> JP6</div> <div> JP7</div> <div> JP8</div>	<div>1 2</div> <div> JP9</div> <div> JP10</div> <div> JP11</div> <div> JP12</div> <div> JP13</div>		<div>1 2</div> <div> JP2</div> <div> JP3</div> <div> JP4</div> <div> JP6</div> <div> JP7</div> <div> JP8</div>	<div>1 2</div> <div> JP9</div> <div> JP10</div> <div> JP11</div> <div> JP12</div> <div> JP13</div>

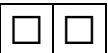
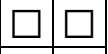


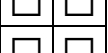
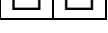




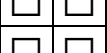
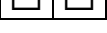




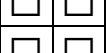
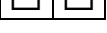
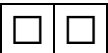



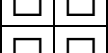

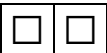



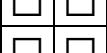

CPU TYPE	JP2~4, JP6~8	JP9 ~ JP13
Intel 80503-233	66MHz x 3.5	V _{CORE} = 2.8V
	<div>1 2</div> <div> JP2</div> <div> JP3</div> <div> JP4</div> <div> JP6</div> <div> JP7</div> <div> JP8</div>	<div>1 2</div> <div> JP9</div> <div> JP10</div> <div> JP11</div> <div> JP12</div> <div> JP13</div>

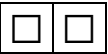
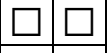
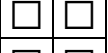
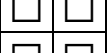
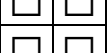
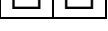



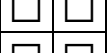
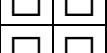
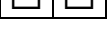



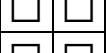
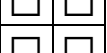
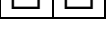
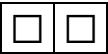


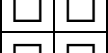
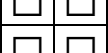

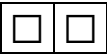


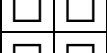
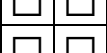
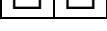
(D) OTHER CPU CLOCK SETTING RESERVED ON THE BOARD :

66MHz x 5	66MHz x 5.5	75MHz x 3.5	75MHz x 4	75MHz x 4.5
<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input type="checkbox"/> <input type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>





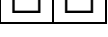









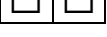









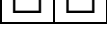
75MHz x 5	75MHz x 5.5	83MHz x 3	83MHz x 3.5	83MHz x 4
<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input type="checkbox"/> <input type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input type="checkbox"/> <input type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>









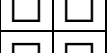


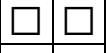




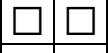
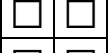



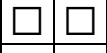
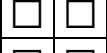
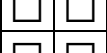

83MHz x 4.5	83MHz x 5	83MHz x 5.5	95MHz x 2.5	95MHz x 3
<div>1 2</div> <div> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input type="checkbox"/> <input type="checkbox"/> JP3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP4 <input type="checkbox"/> <input type="checkbox"/> JP6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input type="checkbox"/> <input type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input type="checkbox"/> <input type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>	<div>1 2</div> <div> <input type="checkbox"/> <input type="checkbox"/> JP2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP3 <input type="checkbox"/> <input type="checkbox"/> JP4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP6 <input type="checkbox"/> <input type="checkbox"/> JP7 <input type="checkbox"/> <input type="checkbox"/> JP8 </div>

95MHz x 3.5	95MHz x 4	95MHz x 4.5	95MHz x 5	95MHz x 5.5
1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8

100MHz x 3.5	100MHz x 4	100MHz x 4.5	100MHz x 5	100MHz x 5.5
1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8	1 2  JP2  JP3  JP4  JP6  JP7  JP8

(E) OTHER CPU VOLTAGE SETTING RESERVED ON THE BOARD:

V _{CORE} = 3.4V	V _{CORE} = 3.1V	V _{CORE} = 3.0V	V _{CORE} = 2.7V	V _{CORE} = 2.6V
1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13

V _{CORE} = 2.5V	V _{CORE} = 2.4V	V _{CORE} = 2.3V	V _{CORE} = 2.1V	V _{CORE} = 2.0V
1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13	1 2  JP9  JP10  JP11  JP12  JP13

V _{CORE} = 1.9V	V _{CORE} = 1.8V	V _{CORE} = 1.7V	V _{CORE} = 1.6V
<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP9</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP10</div> <div><input type="checkbox"/> <input type="checkbox"/> JP11</div> <div><input type="checkbox"/> <input type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>	<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP9</div> <div><input type="checkbox"/> <input type="checkbox"/> JP10</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP11</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP12</div> <div><input type="checkbox"/> <input type="checkbox"/> JP13</div>

(F) JP5 DRAM Clock selection

JP5	SDRAM CLOCK SELECT
<div>1 2</div> <div><input type="checkbox"/> <input type="checkbox"/> JP5</div>	SDRAM CLOCK = CPU CLOCK
<div>1 2</div> <div><input checked="" type="checkbox"/> <input checked="" type="checkbox"/> JP5</div>	SDRAM CLOCK = AGP CLOCK

(G) Cross-reference of all frequencies:

CPU Clk	AGP Clk	PCI Clk	SDRAM Clock JP5=Short	SDRAM Clock JP5=Open	JP6	JP7	JP8
60MHz	60MHz	30MHz	60MHz	60MHz	Short	Short	Short
66.8MHz	66.8MHz	33.4MHz	66.8MHz	66.8MHz	Open	Short	Short
75MHz	75MHz	37.5MHz	75MHz	75MHz	Open	Open	Short
75MHz	60MHz	30MHz	60MHz	75MHz	Short	Short	Open
83.3MHz	66.6MHz	33.3MHz	66.6MHz	83.3MHz	Open	Short	Open
95.2MHz	63.5MHz	31.75MHz	63.5MHz	95.2MHz	Short	Open	Open
100MHz	66.6MHz	33.3MHz	66.6MHz	100MHz	Open	Open	Open

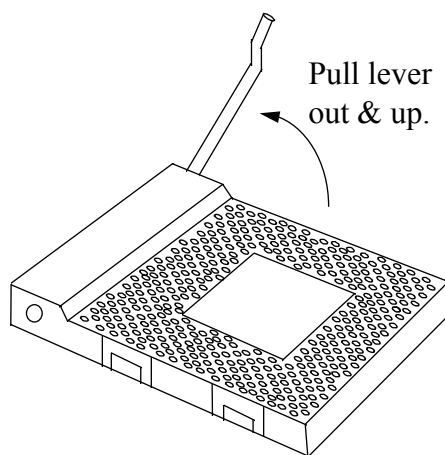
3.3 INSTALLING A CPU ONTO THE ZIF SOCKET

The ZIP type Socket for CPU is the so called Socket 7. It is designed for the Pentium™

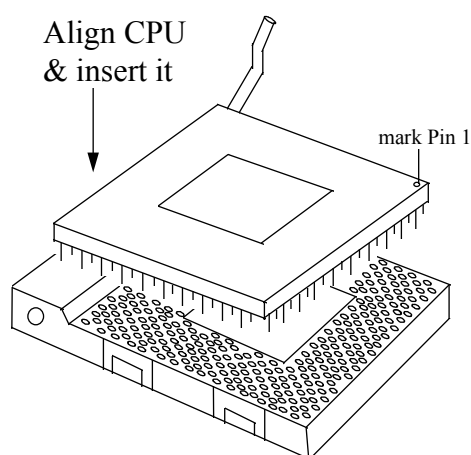
or other equivalent processors. When inserting the Pentium™ processor onto the Socket 7, certain precautionary steps must be followed. The following diagrams will show you how to install the CPU step by step.

1. Make sure the ZIF socket level is up.

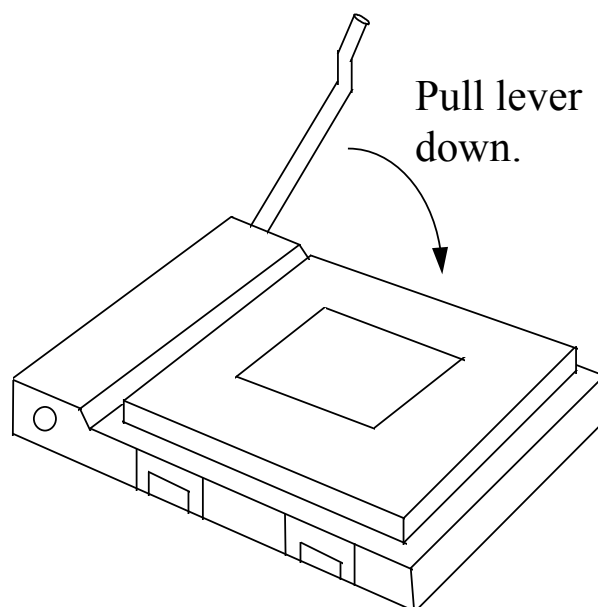
To raise the lever, pull it out to the side a little and raise it as far as it will go. Pin 1 is at the arm corner.



2. Align the CPU and socket pin 1 corners. Match the processor corner containing the blunt edge and the white dot to the socket corner with the distinctive pin arrangement. The pins on the bottom should have aligned with the inner 3 rings of holes in the socket. Place the CPU into the socket and it will go into the socket easily. If it won't, pull the level up a little more and try again.



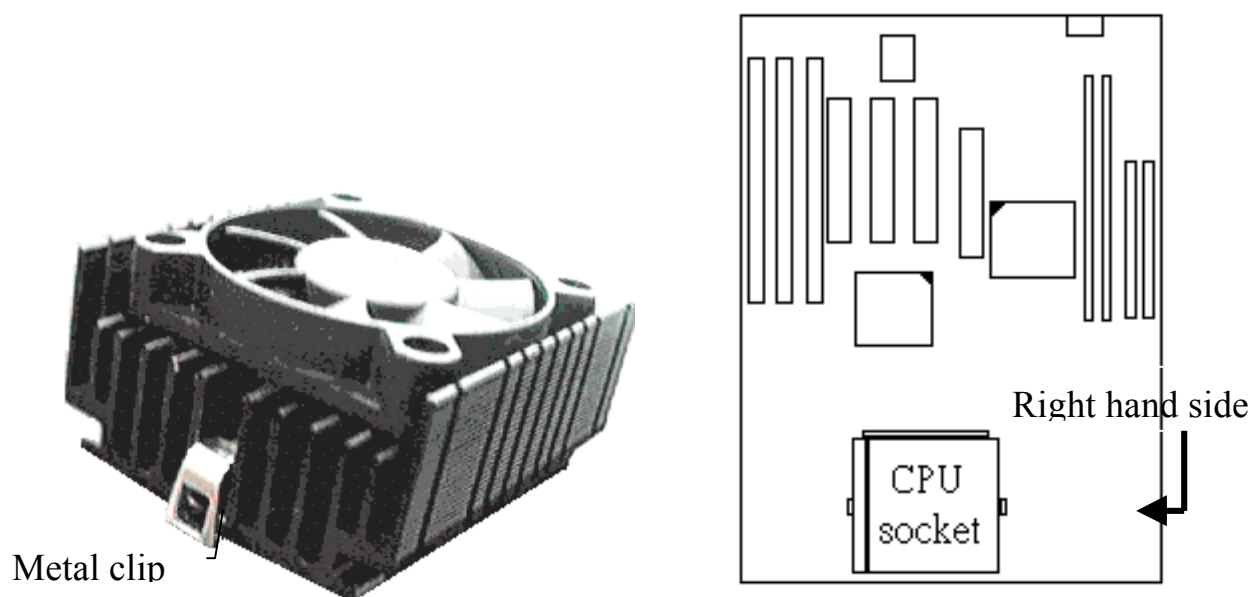
3. Press the lever down. The plate will slide forward. You will feel some resistance as the pressure starts to secure the CPU in the socket. When the CPU is installed, the lever will snap into place at the side of the socket.



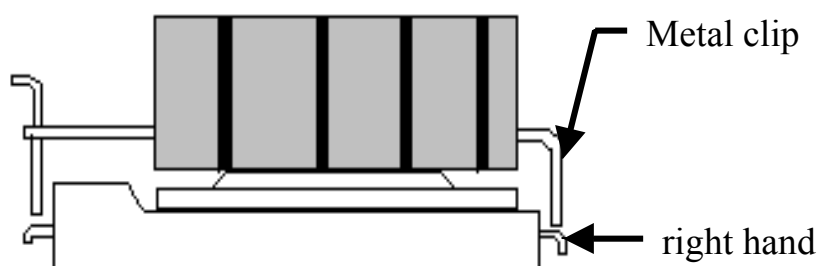
3.4 INSTALLATION OF CPU COOLING FAN

Improper installation of CPU cooling fan may cause serious damage to the motherboard. Please follow the procedures carefully:

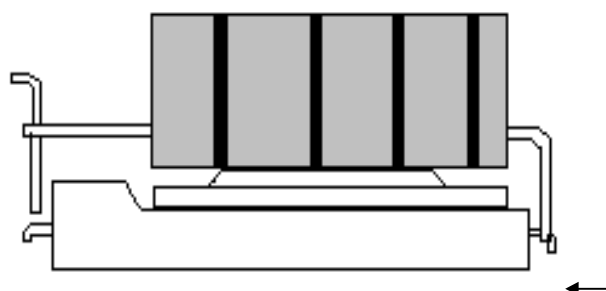
1. There is a metal clip attached to the CPU cooler as shown below.



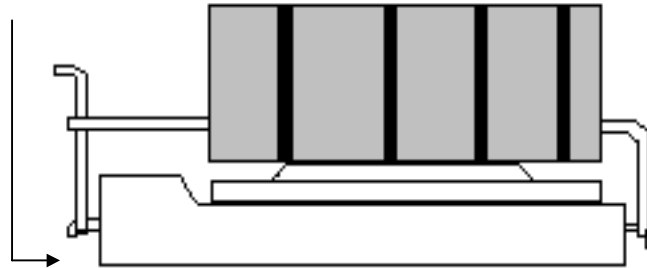
2. Place the CPU cooler squarely on the top of CPU.



3. Hook the right hand side clip to the CPU socket first.

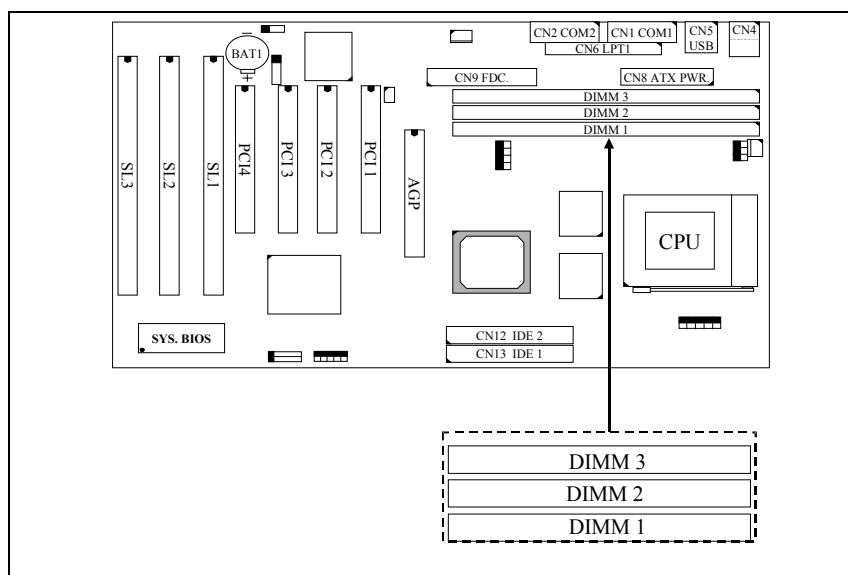


4. Push down the opposite side of the metal clip firmly and carefully to lock the cooler in place.



3.5 INSTALL THE SYSTEM MEMORY

This mainboard supports three 168-pin DIMM sockets (DIMM1, DIMM2 and DIMM3), each DIMM can be single-density or double-density, 8MB up to 1GB of local memory can be installed on the mainboard. It supports two types of DRAM memory, it can be either the Extended Data Out (EDO) or Synchronous (SDRAM) memory. (Both Symmetrical and Asymmetrical DRAM addressing are supported.) The recommended DIMM modules must be **3.3V**, unbuffered and DRAMs' speed must be 60ns or 70ns,.



Picture of DRAM sub-system

In order to increase of the system performance, please avoid populating EDO DIMM module and SDRAM DIMM module on the mainboard at the same time.

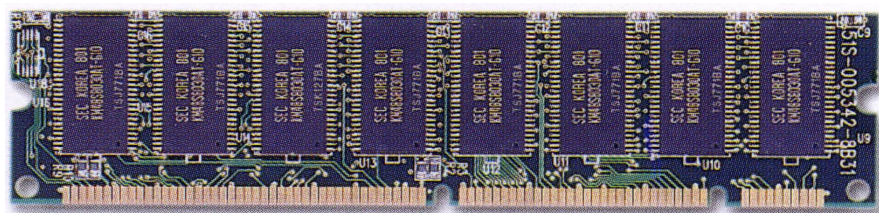
In the DRAM subsystem, the ECC feature is supported by the mainboard and it will check on the DRAM interface (Functions selected by BIOS via CMOS setup, please refer to section 4-5, the default status is Non-ECC selected.) All DIMMs must be populated with true *parity bit* to implement ECC functions.

The ECC is an optional data integrity feature provided by the mainboard and the processor. This feature provides single-bit error correction, multiple-bit error detection, and detection of all errors confined to single nibble for DRAM memory subsystem.

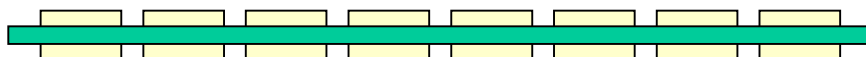
***** Please make sure to use the 3.3V DIMM modules on the mainboard.. *****

Installation of DIMM modules:

1.Outlook of DIMM modules:



(Single-Side DIMM Module)



(Double-Side DIMM Module)

2. Minimum one DIMM module must be installed on the mainboard.
3. You can use single side or double side DIMM module on this mainboard.
4. If you are using 66MHz CPU, please use 3.3V PC-66 or PC-100 DIMM module.
5. If you are using 100MHz CPU, please use 3.3V PC-100 DIMM module..
6. Please install the DIMM module starting from DIMM1 or DIMM2 first.

4. AWARD BIOS SETUP

4.1 GETTING STARTED

When the system is powered on or reset, the BIOS will execute the Power-On Self Test routines (POST) and checks the functionality of every component in the PC system. During the POST, you will see a copyright message on the screen followed by a diagnostics and initialization procedure. (If an EGA or VGA card is installed, the copyright message of the video card maybe displayed on the screen first.) When the system detects any error, it will gives a series of beeping sounds or display the error message on your screen. Basically, the following screen will be displayed when the system is powered on:

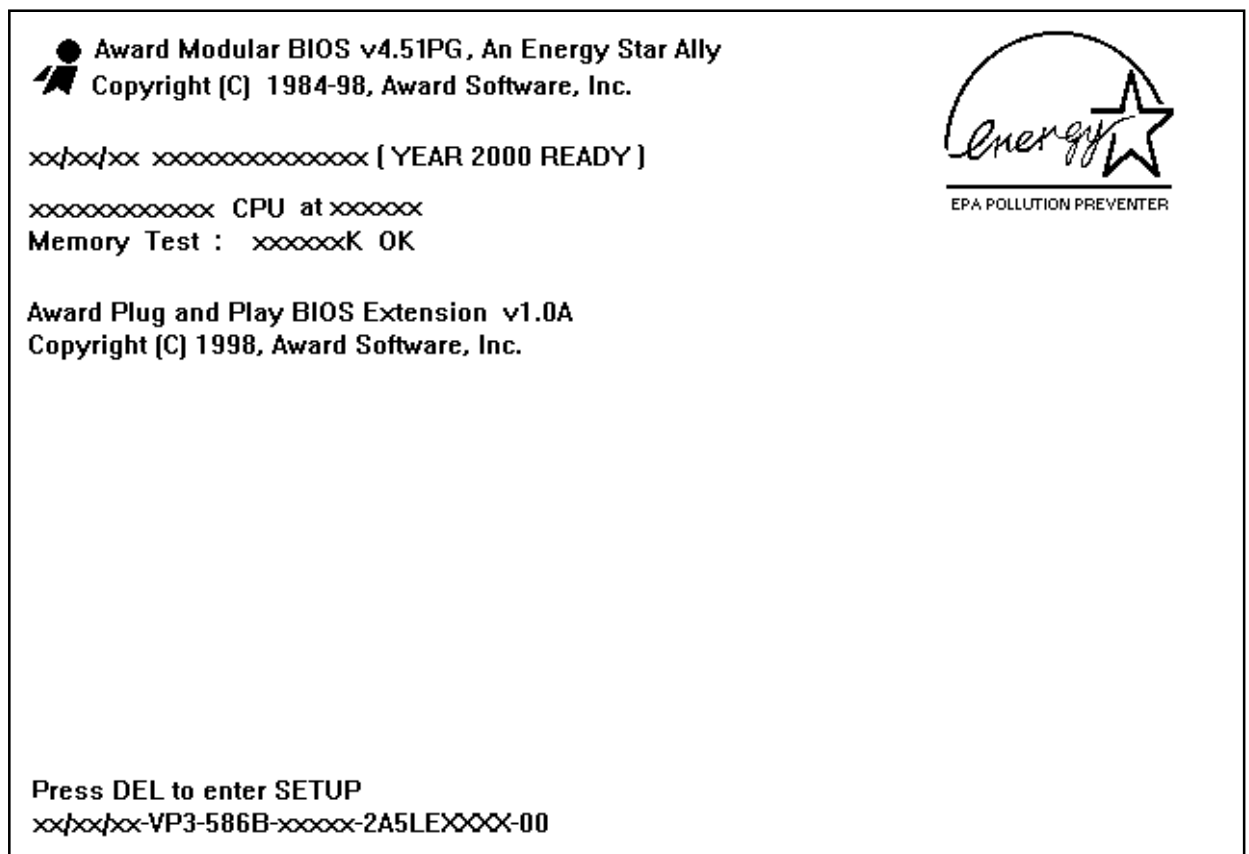


Fig. 4-1 Initial Power-On screen.

After the POST routines are completed, you will find the following message appears on the lower-left screen :

“ Press **DEL** to enter SETUP ”

To execute the Award BIOS Setup program, press the **DEL** key and the “MAIN MENU” of the BIOS setup utility as shown in Fig 4-2 will be triggered.

4.2 MAIN MENU

ROM PCI / ISA BIOS (2A5LEXXX)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	SUPERVISOR PASSWORD
BIOS FEATURES SETUP	USER PASSWORD
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PNP/PCI CONFIGURATION	EXIT WITHOUT SAVING
INTEGRATED PERIPHERALS	
LOAD SETUP DEFAULTS	
ESC : Quit	↑↓←→ : Select Item
F10 : Save & Exit Setup	(Shift)F2 : Change Color
Time, Date, Hard Disk Type ...	

Fig. 4-2 CMOS SETUP MAIN MENU screen.

4.3 CONTROL KEYS

Listed below is an explanation of the keys displayed at the bottom of the screens which will be used in the BIOS SETUP program :

Arrow Keys	: Use the arrow keys to move the cursor to the desired item.
Enter	: To select the desired item.
F1	: Display the help screen for the selected feature.
(Shift)F2	: To change the screen color, total 16 colors.
ESC	: Exit to the previous screen.
PgUp(-)/PgDn(+)	: To modify or change the default value of the highlighted item.
F7	: Loads the SETUP default values from BIOS default table, (only for the current page will be recovered)
F10	: Save all changes made to CMOS RAM in the MAIN MENU.

The following sections shows all the screens which you will find in the CMOS SETUP routine, each screen contains the selection options and its default settings. At the bottom of some screen display, you may find the description of all function key which you can use it to change the settings. If you are not quite sure of the definition for some specific items, please consult your mainboard supplier for details.

4.4 STANDARD CMOS SETUP

ROM PCI / ISA BIOS (2A5LEXXX)

STANDARD CMOS SETUP

AWARD SOFTWARE, INC.

Date (mm : dd : yy)	Fri	Jul	17	1998						
Time (hh : mm : ss)	9	:	6	:	45					
HARD DISKS	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE		
Primary Master	Auto	0	0	0	0	0	0	Auto		
Primary Slave	None	0	0	0	0	0	0	-----		
Secondary Master	Auto	0	0	0	0	0	0	Auto		
Secondary	None	0	0	0	0	0	0	-----		
Drive A : 1.44M, 3.5 in.					<div style="border: 1px solid black; padding: 5px;"> Base Memory : 640 K Extended Memory : xxxxxx K Other Memory : xxxxxx K <hr/> Total Memory : xxxxxx K </div>					
Drive B : None										
Video : EGA/VGA										
Halt On : All Errors										
ESC : Quit					↑↓←→ : Select Item		PU/PD/+/- : Modify			
F1 : Help					(Shift)F2 : Change Color					

Fig. 4-3 STANDARD CMOS SETUP screen.

MODE:

The BIOS on the mainboard is the updated one and which provides three different modes to support both normal size IDE hard disk drive and the hard disk drive above 528MB:

- **NORMAL** : For IDE hard disk drives which is smaller than 528MB.
- **LBA** : For IDE hard disk drive which is above 528MB (ideally, it can be as big as 8.4GB) that use Logic Block Addressing (LBA) mode.
- **Large** : For IDE hard disks size larger then 528MB but it does not support the LBA mode.

Note: Large mode is a new technology and it is not fully supported by most operation systems so far. So only MS-DOS is recommended on such hard disk drive. Fortunately, such hard disk drive is not very common nowadays.

Note : Some certain operation system (like SCO-UNIX) will have to choose the "NORMAL" mode when installation.

4.5 BIOS FEATURES SETUP

ROM PCI / ISA BIOS (2A5LEXXX)

BIOS FEATURES SETUP

AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
External Cache	: Enabled	CC000-CFFFF Shadow	: Disabled
Quick Power On Self Test	: Enabled	D0000-D3FFF Shadow	: Disabled
Boot Sequence	: A,C,SCSI	D4000-D7FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	DC000-DFFFF Shadow	: Disabled
Boot Up NumLock Status	: On		
Gate A20 Option	: Normal		
Memory Parity/ECC Check	: Enabled		
Typematic Rate Setting	: Disabled		
Typematic Rate (Chars/Sec)	: 6		
Typematic Delay (Msec)	: 250		
Security Option	: Setup		
IDE Second Channel Control	: Enabled		
PS/2 mouse function control	: Enabled	ESC : Quit	↑↓←→ : Select Item
PCI/VGA Palette Snoop	: Disabled	F1 : Help	PU/PD/+/- : Modify
OS Select For DRAM>64MB	: Non-OS2	F5 : Old Values (Shift)	F2 : Color
Report No FDD For WIN95	: No	F7 : Load Setup Defaults	

Fig. 4-4 BIOS FEATURES SETUP screen.

Virus Warning : (Default values is “Disabled”)

In order to avoid virus infection happens on your PC system, this mainboard provides the virus warning features in the BIOS. During and after the operation system is loaded, any attempt to write to the boot sector or partition table on the IDE hard disk drive will trigger this feature and give you some warning messages on the screen and then halt the system. When you find the message on your screen, please run an anti-virus program to see whether your system is infected by a virus or not.

Enabled : Activate automatically when the system boots up causing a warning message to appear on the screen when anything attempts to access the boot sector of the hard disk partition table.

Disabled : No warning message to appear when anything attempts to access the boot sector or hard disk partition table.

CPU Internal Cache :

This option enables CPU's internal (L1) cache memory. If you want to use the internal (L1) cache memory and external (L2) cache memory, you may use this option to enable or disable the setting.

External Cache :

This option enables L2 (secondary) external cache memory. If there is no external cache memory on board you have to select “disabled”,

4.6 CHIPSET FEATURES SETUP

ROM PCI / ISA BIOS (2A5LEXXX)

CMOS SETUP UTILITY

CHIPSET FEATURES SETUP

Bank 0/1 DRAM Timing	: SDRAM 10ns	OnChip USB	: Disabled
Bank 2/3 DRAM Timing	: FP/EDO 70ns	USB Keyboard Support	: Disabled
Bank 4/5 DRAM Timing	: FP/EDO 70ns		
SDRAM Cycle Length	: 3	Auto Detect DIMM/PCI CLK	: Enabled
DRAM Read Pipeline	: Enabled	Spread Spectrum	: Disabled
Cache Rd+CPU Wt Pipeline	: Enabled		
Cache Timing	: Fast		
Video BIOS Cacheable	: Enabled		
System BIOS Cacheable	: Enabled		
Memory Hole At 15Mb Addr.	: Disabled		
AGP Aperture Size	: 64M		
		ESC : Quit	↑↓←→ : Select Item
		F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift)F2 : Color
		F7 : Load Setup Defaults	

Fig. 4-5 CHIPSET FEATURES SETUP screen.

WARNING : The selection fields on this screen are provided for the professional technician who can modify the Chipset features to meet some specific requirement. If you do not have the related technical background, do not attempt to make any change except the following items.

Bank 0/1 (2/3, 4/5)DRAM Timing :

BANK 0/1: DIMM1

BANK 2/3: DIMM2

BANK 4/5: DIMM3

The memory modules inserted onto the memory subsystem will be detected by the system BIOS automatically. For example, when you insert a SDRAM module onto the DIMM sockets, “SDRAM 10ns” will be displayed on the screen shown above. (It will be “FP/EDO 70ns” when SDRAM module is absent on the DIMM subsystem.) There are two optimum values suggested for the chipset and CPU registers. You may select either 60ns or 70ns for EDO modules. Basically, “60 ns” will let you have better performance. However, “70ns” is recommended in most case causes it works with most EDO DRAM modules, As for SDRAM modules, “10ns” is suggested for most modules. “8ns” will let you have begtter performance, but it may cause system unstable when SDRAM modules are not fast enough.

4.7 POWER MANAGEMENT SETUP

ROM PCI / ISA BIOS (2A5LEXXX)

POWER MANAGEMENT SETUP

AWARD SOFTWARE, INC.

Power Management	: User Define	Primary INTR	: ON
PM Control by APM	: Yes	IRQ3 (COM 2)	: Primary
Video Off Option	: Suspend->Off	IRQ4 (COM 1)	: Primary
Video Off Method	: Blank Screen	IRQ5 (LPT2)	: Primary
MODEM Use IRQ	: 3	IRQ6 (Floppy Disk)	: Primary
Soft-Off by PWRBTN	: Instant-Off.	IRQ7 (LPT1)	: Primary
** PM Timers **		IRQ8 (RTC Alarm)	: Disabled
HDD Power Down	: Disabled	IRQ9 (IRQ2 Redir)	: Secondary
Doze Mode	: Disabled	IRQ10 (Reserved)	: Secondary
Suspend Mode	: Disabled	IRQ11 (Reserved)	: Secondary
** PM Events **		IRQ12 (PS/2 Mouse)	: Primary
VGA	: OFF	IRQ13 (Coprocessor)	: Primary
LPT & COM	: LPT/COM	IRQ14 (Hard Disk)	: Primary
HDD & FDD	: ON	IRQ15 (Reserved)	: Disabled
DMA/master	: OFF		
Modem or LAN Resume	: Disabled	ESC : Quit	↑↓←→ : Select Item
RTC Alarm Resume	: Disabled	F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift)F2 : Color
		F7 : Load Setup Defaults	

Fig. 4-6 POWER MANAGEMENT SETUP screen.

WARNING : The selection fields on this screen are provided for the professional technician who can modify the Chipset features to meet some specific requirement. If you do not have the related technical background, do not attempt to make any change except the following items.

Power management :

This setting controls the Power Management functions. “User Define” will allow user to define his own parameters. “Min Saving” and “Max Saving” is a quick selection option which will fix the values of four parameters, including “Doze Mode”, “Suspend Mode” and “HDD Power Down”. When “Disable” is selected, it will disable all Power Management functions.

4.8 PNP/PCI CONFIGURATION

ROM PCI / ISA BIOS (2A5LEXXX)

PNP/PCI CONFIGURATION

AWARD SOFTWARE, INC.

PNP OS Installed	: No	CPU to PCI Write Buffer	: Enabled
Resources Controlled By	: Manual	PCI Dynamic Bursting	: Enabled
Reset Configuration Data	: Disabled	PCI Master 0 WS Write	: Enabled
ACPI I/O Device Node	: Enabled	PCI Delay Transaction	: Enabled
IRQ-3 assigned to	: PCI/ISA PnP	PCI Master Read Prefetch	: Enabled
IRQ-4 assigned to	: PCI/ISA PnP	PCI #2 Access #1 Retry	: Disabled
IRQ-5 assigned to	: PCI/ISA PnP	AGP Master 1 WS Write	: Enabled
IRQ-7 assigned to	: PCI/ISA PnP	AGP Master 1 WS Read	: Disabled
IRQ-9 assigned to	: PCI/ISA PnP		
IRQ-10 assigned to	: PCI/ISA PnP	PCI IRQ Activated By	: Level
IRQ-11 assigned to	: PCI/ISA PnP	Assign IRQ For USB	: Enabled
IRQ-12 assigned to	: PCI/ISA PnP	Assign IRQ For VGA	: Enabled
IRQ-14 assigned to	: PCI/ISA PnP		
IRQ-15 assigned to	: PCI/ISA PnP		
DMA-0 assigned to	: PCI/ISA PnP		
DMA-1 assigned to	: PCI/ISA PnP	ESC : Quit	↑↓←→ : Select Item
DMA-3 assigned to	: PCI/ISA PnP	F1 : Help	PU/PD/+/- : Modify
DMA-5 assigned to	: PCI/ISA PnP	F5 : Old Values	(Shift)F2 : Color
DMA-6 assigned to	: PCI/ISA PnP	F7 : Load Setup Defaults	
DMA-7 assigned to	: PCI/ISA PnP		

Fig. 4-7 PNP/PCI CONFIGURATION setup screen.

WARNING : The selection fields on this screen are provided for the professional technician who can modify the Chipset features to meet some specific requirement. If you do not have the related technical background, do not attempt to make any change except the following items.

Resources Controlled by :

- Manual :** The system BIOS will not refer to the ESCD data to assign IRQ & DMA. Instead, it will refer to the information recorded in this field when assigning the IRQ & DMA resource. (Anyhow, the system BIOS will always refer to the ESCD data to assign the I/O and memory space resources).
- Auto :** The system BIOS will refer to the ESCD segment for all legacy information.

Reset Configuration Data :

Disabled: The system BIOS will do nothing.

Enabled : The system BIOS will clear/reset the ESCD during “POST”. After clearing the ESCD, the system BIOS will then change this item’s value back to “Disable”, otherwise, the ESCD will become useless.

There are only 15 IRQs and 8 DMAs available on the mainboard and most of them are assigned for some specific purposes. Sometimes, user may feel like to have some more IRQ and DMA in order to install the new add on cards. In this case, you may use this field to assign some certain IRQ and DMA to “PCI/ISA PnP” so that the new add on card will find the free IRQ or DMA available for it.

Legacy : The system BIOS will skip and never assign the specified IRQ/DMA resource to PCI or ISA PnP devices and the IRQ and DMA can only be used by their specified Legacy ISA cards.

PCI/ISA: When the “PCI/ISA PnP” is been selected, the related IRQ and DMA will be released and they can be used by other PCI or ISA devices. Whenever there is the new PCI or ISA devices plugged onto the mainboard, the system BIOS will detect it and assign a free IRQ or DMA for the new devices.

Note: Most IRQ and DMA have its own purpose and they can not be assigned to “PCI/ISA PnP”. For example, IRQ14 and IRQ15 are used by the onboard IDE device. If you change the setting on IRQ14 and IRQ15, you will be unable to connect the hard disk drive or CD-ROM drive to the IDE interface on the mainboard. So please make sure to check the IRQ and DMA assignment in your system before you proceed to do the setting. For instance, if you do not have the printer (IRQ7) or PS/2™ mouse (IRQ12) connected to your PC system, you may assign IRQ7 and IRQ12 to “PCI/ISA PnP” so that you can have more IRQs available for new add on cards.

Explanation for technical issue:

PnP device :

- Device that has Plug & Play compatibility. That means it will request for DMA, IRQ, I/O and Memory from the PnP BIOS and all these requests can be re-locatable. In other words, these devices do not utilize any fixed resources.
- All PCI devices and all ISA PnP devices are PnP devices.

Legacy device :

- A legacy device is a device that all its resources are fixed by hardware (or selected by jumpers).
- All ISA Non-PnP devices are legacy device.

Extended System Configuration Data (ESCD) :

- A media between the user and the system BIOS for passing the legacy devices information's. This information is stored in the onboard NVRAM (flash ROM).

4.9 INTEGRATED PERIPHERALS

ROM PCI / ISA BIOS (2A5LEXXX)

INTEGRATED PERIPHERALS

AWARD SOFTWARE, INC.

On-Chip IDE First Channel	: Enabled	Onboard Parallel Port	: 378 / IRQ 7
On-Chip IDE Second Channel	: Enabled	Onboard Parallel Mode	: SPP
IDE Prefetch Mode	: Enabled		
IDE HDD Block Mode	: Enabled		
IDE Primary Master PIO	: Auto		
IDE Primary Slave PIO	: Auto		
IDE Secondary Master PIO	: Auto		
IDE Secondary Slave PIO	: Auto		
IDE Primary Master UDMA	: Auto		
IDE Primary Slave UDMA	: Auto		
IDE Secondary Master UDMA	: Auto		
IDE Secondary Slave UDMA	: Auto		
Init Display First	: PCI Slot		
Onboard FDC Controller	: Enabled		
Onboard Serial Port 1	: 3F8 / IRQ 4	ESC : Quit	↑↓←→ : Select Item
Onboard Serial Port 2	: 2F8 / IRQ 3	F1 : Help	PU/PD/+/- : Modify
UART 2 Mode	: Standard	F5 : Old Values	(Shift)F2 : Color
		F7 : Load Setup Defaults	

Fig. 4-8 INTEGRATED PERIPHERALS setup screen.

WARNING : *The selection fields on this screen are provided for the professional technician who can modify the Chipset features to meet some specific requirement. If you do not have the related technical background, do not attempt to make any change except the following items.*

UART 2 Mode :

This setting determines the IR port (CN7) function mode. Supports both HPSIR and ASKIR.

Onboard Parallel Mode :

This setting determines the onboard parallel port (CN6) transmission mode. Supports either SPP, EPP, ECP, or ECP+EPP.

4.10 LOAD SETUP DEFAULTS

If you lost the CMOS data or you don't know how to complete the setup procedure, you may use this option to load the SETUP default values from the BIOS default table. It is easy to load the default value, simply highlight the "LOAD SETUP DEFAULTS" field and then press the "Enter" key, when you see the "LOAD SETUP DEFAULTS (Y/N)" displayed on the screen, response to it with "Y" and then press the "Enter" key. The SETUP default values will be loaded. Basically, the SETUP default settings are the best-case values that will optimize system performance and increase system stability.

In case that the CMOS data is corrupted, the SETUP DEFAULTS settings will be loaded automatically when you press the "Del" key and enter the main setup screen. So you may select "SAVE & EXIT SETUP" to leave setup program and the system is loaded with the default settings.

4.11 SUPERVISOR PASSWORD / USER PASSWORD

The "SUPERVISOR PASSWORD" and "USER PASSWORD" will be used to check the authority when power-on. Whenever there is the password stored in either of these fields, the correct password will be requested so that the PC system will continue to load the operation system.

You can enter up to eight alphanumeric characters here. When you have typed in the password and pressed the "Enter" key, you will be asked to reconfirm your password again to complete password setup. If you press the "Enter" key twice without any alphanumeric character entered, the PASSWORD will be disabled.

If the "User Password" and the "Supervisor Password" are both enabled and they have different password setup, "Supervisor Password" is always has the higher priority, Basically, an "User" is only authorized to change the content of "User Password", while a "Supervisor" has the authorization to dominate all settings.

4.12 IDE HDD AUTO DETECTION

In order to make the IDE hard disk known to the system, you need to tell the system what kind of hard disk is connected to the mainboard by giving a set of hard disk parameters. Sometimes it is not easy for users to find the proper parameters for their IDE hard disk drive. In order to help users to find the parameters, the system BIOS provides a convent way – the auto detection of IDE hard disk drive.

To run the auto detection program is extremely easy. Move the selection bar to “IDE HDD AUTO DETECTION” and then press “Enter”, the system BIOS take over the job and try to detect the type of IDE hard disk. If it succeeds, you will see a list of hard disk with its related parameters. You may press on the “Y” key (or select one of the hard disk type listed on the screen). The system BIOS will transfer the parameters to the corresponding fields in the STANDARD CMOS SETUP menu and you have completed the IDE hard disk setup.

4.13 SAVE &EXIT SETUP

This option will save all setup values to CMOS RAM & EXIT SETUP routine, by moving the selection bar to “SAVE & EXIT SETUP” and pressing “Enter” key, then types “Y” and “Enter” key, the values will be saved and all the information will be stored in the CMOS memory, and then the setup program will be terminated and the system will start to reboot.

4.14 EXIT WITHOUT SAVING

This item exit the setup routine without saving any changed values to CMOS RAM, When you do not want to save your change to the CMOS memory, you may choose to run this option and the setting what you made in the BIOS setup routine will be given away.

Move the selection bar to “EXIT WITHOUT SAVING” and click on the “Enter” key, then you will be asked to confirm the action to exit, press the “Y” and “Enter” key, the setup program will be terminated and the system will start to reboot.

