# 1 Introduction

TR5510 AIO is a IBM PC/AT compatible mainboard based on the Intel 430FX PCIset, and UMC8669 Plug and Play Super AT I/O controller. Other on-board specifications include 3 AT Bus slots, 4 PCI Bus slots, 2 memory banks support memory size up to 128MB, and 256/512KB cache memory size.

## General Specifications

| | |
|---|---|
| **Processor:** | Intel Pentium P54C 75/90/100/120/133/150/166 MHz, P54CT, P54CTB<br>Future CPU at 50/60/66 MHz host clock speed<br>Cyrix 6X86 - P120+, P133+, P150+, P166+ |
| **Chipset:** | Intel 430FX PCIset<br>UMC UM8667 (I/O TTL Integration)<br>UM8669 (Plug and Play Super AT I/O) or SMC669 (Optional) |
| **System BIOS:** | Award (128K Flash ROM) |
| **System Memory:** | Supports two banks of DRAM with memory size up to 128MB. All support double side SIMM. |
| **External Cache:** | Write-back architecture.<br>Either on-board asyncronous standard SRAM or one Cache module slot for synchronous Pipelined Burst SRAM supports 256 or 512 KB cache size. |
| **Slots:** | 3 AT-Bus slots<br>4 PCI slots<br>1 Cache Module slot |
| **I/O Connectors:** | Two Serial Ports (16550 compatible UARTs)<br>One Parallel Port (Standard/ECP/EPP)<br>One FDC Connector (360K, 720K, 1.2MB, 1.44MB, or 2.88MB)<br>Two PCI IDE Connectors (support 4 fast IDE interface with DMA or PIO transfer)<br>One AT Keyboard Connector (or PS/2 Keyboard Connector) |
| **Form Factor:** | 3/4 Baby AT |
| **PCB:** | 4 layers |

# Features

- **CPU:**
  - ZIF socket 7 with VRM connector (optional) supports Intel standard/ VRE/VRM Pentium™ P54C 75/90/100/120/133/150/166 MHz,P54CT, P54CTB CPU or future CPU at 50/60/66 MHz host clock speed.
    Cyrix 6X86 - P120+, P133+, P150+, P166+ CPU.

- **BIOS:**
  - Award BIOS with Flash ROM support.
    - PNP specification V1.0a
    - APM specification V1.1
    - PCI specification V2.0
    - CD-ROM boot.

- **Memory:**
  - Four pieces of 72-pin SIMM sockets with memory size from 4MB to 128MB. All support double side SIMMs.
  - EDO/Hyper page mode (X-2-2-2 reads) or standard page mode DRAMs (X-3-3-3 reads) support.
  - 4 Qword deep buffer for 3-1-1-1 posted write cycles.
  - Supports symmetrical and asymmetrical DRAMs.

- **Cache:**
  - Supports the write-back architecture for CPU's internal first level (L1) cache and external secondary level (L2) cache.
    - 256KB or 512KB L2 cache size is supported by:
      On-board asynchronous standard SRAM or
      One slot for synchronous Pipelined Burst SRAM module.
    - Direct mapped organization.
    - Cache hit read/write cycle timings at 3-1-1-1 with Pipelined Burst SRAM's.
    - Back-to-Back read cycles at 3-1-1-1-1-1-1-1 with Pipelined Burst SRAM's.

- **RTC:** Uses Dallas 12887A compatible RTC module (Internal 128 byte of CMOS RAM).

- **Slots:**
  - 3 16-bit ISA slots with 100% ISA compatible functions.
  - 4 32-bit PCI slots support PCI master.
    - PCI specification version 2.0.
    - CPU to PCI memory write posting with 4 Word deep buffers.
    - Converts Back-to-Back sequential CPU to PCI memory writes to PCI Burst writes.
  - One cache module slot supports asynchronous/synchronous Burst and Pipelined Burst SRAM.

- **IDE:**
  - Build-in Intel 430FX PCIset chip 32-bit PCI IDE interface with 2 IDE channels.
  - Supports up to PIO mode 4 timing or DMA mode 2 with transfer rate timing up to 22MB/sec.

- **FDC:**
  - Two floppy drives support 360K, 720K, 1.2M, 1.44M, 2.88M, and 3 mode floppy drives.

- **I/O:**
  - One multi-mode parallel port which include enhanced (EPP) and high speed (ECP) support.
  - Two high speed 16C550 compatible UARTs.

- **Power Management:**
  - Compatible with EPA "Energy-Star" specification.
  - Fully compatible with Microsoft APM V1.1.
  - Supports STOPCLK & SUSPEND function for Intel Pentium CPU.
  - Programmable idle detector including one programmable I/O & one memory region.
  - Suspend/Resume function support.
  - Supports 4 power management modes: Full-on, Doze, Standby, and Suspend modes.

This Page Intentionally Left Blank.