Advanced/AS Motherboard Specification Update

Release Date: August 1997

Order Number: 281824-004

The Advanced/AS motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Date of Revision	Version	Description
August 1996	-001	This document is the first Specification Update for the Intel Advanced/AS motherboard.
December 1996	-002	Added Errata 4-5.
April 1997	-003	Added Errata 6-8, Documentation Change 1 and PBA/BIOS Table.
August 1997	-004	Added Erratum 9, Specification Change 2 and Documentation Changes 2-3.

PREFACE

This document is an update to the specifications contained in the *Advanced/AS Motherboard Technical Product Specification* (Order Number 281836). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium processor. Items contained in the *Pentium Processor Specification Update* that either do not apply to the Advanced/AS motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430FX PCIset Specification Update* (Order Number 297733) for specification updates concerning the 82430FX PCIset. Items contained in the *82430FX PCIset Specification Update* that either do not apply to the Advanced/AS motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the Advanced/AS motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for Advanced/AS Motherboards

GENERAL INFORMATION

Basic Advanced/AS Motherboard Identification Information

AA Revision	PBA Revision	82430FX PCISet Stepping	BIOS Revision	Notes
643160-001 643158-001 643159-001 643260-001	641587-203	A2	1.00.03.CL0	1, 2, 4
643160-002 643158-002 643159-002 643260-002	641587-204	A2	1.00.04.CL0	1, 2, 4
652322-001 643158-001 643159-001 643260-001 643310-001	641587-224	A1	1.00.04.CL0	1, 3, 4
643158-002 643159-001 643160-001 643260-001 643310-001 652322-001	641587-245	A2	1.00.04.CL0	1, 2, 4

NOTES:

1. The PBA number is found on a small label on the component side of the board.
2. The 82430FX PCIset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82437FX TSC	A2	SZ999
82438FX TDP (2)	A1	SZ969
82371FB	A1	SZ997

3. The 82430FX PCIset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82437FX TSC	A1	SZ966
82438FX TDP (2)	A1	SZ965
82371FB	A1	SZ964

4. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the Advanced/AS motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71-79, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update.*

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Advanced/AS motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	ERRATA
1	Fixed	Locked PCI cycles do not terminate properly for the 82437FX TSC component A-1 stepping
2	Fixed	CMOS password plus backspace allows system to boot
3	Fixed	Serial mouse activity does not restore display after APM shutdown
4	NoFix	Secondary IDE hard drive size is 0 MB when set to User Definable
5	NoFix	CMOS checksum may be lost If power is cycled during boot
6	NoFix	BIOS does not support no-emulation mode for CD-ROM boot
7	NoFix	Resource conflict with onboard ATI* video
8	NoFix	Slave on secondary IDE channel is not disabled
9	Fixed	BIOS SETUP does not recognize February 29, 2000 as a valid date
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Entering time and date in system setup
2	Doc	Administrator and user passwords
NO.	**PLANS**	**DOCUMENTATION CHANGES**
1	Doc	Revision of “Second Level Cache” section
2	Doc	Revision of “Clear CMOS - Jumper J7F2” section
3	Doc	Revision of “Peripheral Component Interconnect (PCI) PCIset” section

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
641587-203	1.00.03.CL0	2-8
	1.00.04.CL0	3-8
	1.00.05.CL0	4, 5-8
	1.00.06.CL0	4, 5-8
	1.00.07.CL0	4, 5-8
641587-204	1.00.03.CL0‡	2-9
	1.00.04.CL0	3-9
	1.00.05.CL0	4, 5-9
	1.00.06.CL0	4, 5-8
	1.00.07.CL0	4, 5-8
641587-224	1.00.03.CL0‡	1-9
	1.00.04.CL0	1, 3-9
	1.00.05.CL0	1, 4-9
	1.00.06.CL0	1, 4-8
	1.00.07.CL0	1, 4-8
641587-245	1.00.03.CL0‡	2-9
	1.00.04.CL0	3-9
	1.00.05.CL0	4-9
	1.00.06.CL0	4-8
	1.00.07.CL0	4-8

NOTE:

‡ This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

ERRATA

1. Locked PCI Cycles for the A-1 Stepping of the 82437FX TSC Component Do Not Terminate Properly

PROBLEM: With the A-1 stepping of the 82437FX system controller (TSC) component, locked PCI cycles do not terminate properly if the target device signals Retry after the LOCK# signal has been asserted. If another PCI bus master device accesses memory under these conditions, the memory access will never be completed and the system will lock up. This lockup has only been seen with certain VGA* video cards when the video driver uses the XCHG instruction.

IMPLICATION: The system video may lock at certain times with Microsoft Windows* 95 if the default VGA driver is used.

WORKAROUND: Use the alternate Windows 95 VGA driver (named VGA.DRV) found in the \drivers\display\vga directory on the Windows 95 CD-ROM. Copy this into the windows\system directory on the system hard drive.

STATUS: This erratum only affects PBA revision 641587-224.

2. CMOS Password Plus Backspace Allows System to Boot

PROBLEM: After typing the correct password on the command line for the BIOS Setup program, if a backspace is used to delete the last character of the password the system will still boot when enter is pressed.

IMPLICATION: In effect, this allows an incorrect password to be used to boot the system.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.04.CL0.

3. Serial Mouse Activity does not Restore Display After APM Shutdown

PROBLEM: Moving a mouse attached to the serial port of the system will not restore the video display when the system is in a power-down state.

IMPLICATION: The display will not be restored from its APM state until a key is pressed. However, the system will be awakened by the movement of the serial mouse.

WORKAROUND: Use a mouse attached to the PS/2* mouse port in order for the display to be restored. Also, hit any key to restore the system and display from a power-down state.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CL0

4. Secondary IDE Hard Drive Size is 0 MB When Set to User Definable

PROBLEM: Selecting the User Definable option from the Secondary IDE Interface menu in the BIOS Setup program, the maximum capacity of the drive is shown as 0 MB. This value remains unchanged regardless of cylinder, head or sector values.

IMPLICATION: The value shown in the Secondary IDE Interface menu will always be 0 MB. However, the entire drive is accessible and will function normally.

WORKAROUND: Use the Primary IDE Interface for hard drives that require user-definable parameters.

STATUS: This erratum will not be fixed.

5. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte is not updated. The next time the computer is turned on, the message "CMOS Checksum Invalid" will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

> Date and Time Not Set
> Press <F1> for Setup, <Esc> to Boot

is displayed, the user must reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

6. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an "El Torito" bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum will not be fixed.

7. Resource Conflict with Onboard ATI Video*

PROBLEM: The system may fail to initialize a 3COM 3C595 bus mastering network card when configured as a Windows NT 3.51 server or workstation. Windows NT reports that there is a conflict with the resources of the 3COM 3C595 network card and the onboard ATI* video.

IMPLICATION: The resource conflict will not allow the server to logon to the domain controller. Attaching to the network as a workstation may be intermittent.

WORKAROUND: None.

STATUS: This erratum was fixed with revision 3.0 of the ATI Mach64* drivers for Windows NT 3.51 available at http:\\www.intel.com.

8. Slave on Secondary IDE Channel is not Disabled

PROBLEM: If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.
- ATAPI device attached as slave to the secondary IDE connector.

IMPLICATION: In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

9. BIOS SETUP Does Not Recognize February 29, 2000 As a Valid Date

PROBLEM: The BIOS Setup program will not allow the system date to be set to Feb 29, 2000.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: If the system BIOS has not been upgraded, the system date will have to be reset to the correct date on March 1, 2000.

STATUS: This erratum was fixed in BIOS revision 1.00.06.CL0.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Advanced/AS Motherboard Technical Product Specification* (Order Number 281836). All Specification Clarifications will be incorporated into a future version of the appropriate Advanced/AS motherboard documentation.

1. Entering Time And Date In System Setup

The following will be added in Appendix K after paragraph 1 of the subsection *System Time*:

To enter 00:xx:xx, zeros in the hour field, use the following steps.

- Enter some values in the hour fields. For example, enter 21 in the hour fields as follows:

  21:xx:xx

- Use the cursor key to move to the right hour field and change the digit to 0 (zero).

  20:xx:xx

- Move to the left hour field and change the digit to 0 (zero).

  00:xx:xx

2. Administrator and User Passwords

The following will be added to Administrative and User Access Modes:

If an administrator password has been set, but no user password has been set, a user can create a password by entering BIOS Setup at boot by pressing the <F1> key and pressing enter at the administrator password prompt. Once in BIOS Setup, a user will be able to create a new user password.

Once defined, a user password can be cleared by either defining a new user password in Setup, or by moving the Password Clear jumper (J7F1) on the motherboard. See Password Clear Jumper - Jumper J7F1 for more information on how to use this jumper.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Advanced/AS Motherboard Technical Product Specification* (Order Number 281836). All Documentation Changes will be incorporated into a future version of the appropriate Advanced/AS motherboard documentation.

1. Revision of Second Level Cache Section

The first paragraph in this section will be replaced in its entirety as follows:

The processor's internal cache can be complimented by a second level cache using either new high-performance pipeline burst SRAM, or traditional asynchronous SRAM. PB SRAM have registered data outputs. This allows SRAM vendors to use CMOS instead of expensive BiCMOS technology to produce PB SRAM. With the 82430FX PCIset, the performance level of PB and Synchronous SRAM is identical. The Intel PCIset determines the amount of cacheable system memory, for the 82430FX, the first 64 MB of system memory is cacheable.

2. Revision of Clear CMOS - Jumper J7F2 Section

This section will be replaced in its entirety as follows:

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the system on. When the system reports that “NVRAM cleared by jumper”, the system can be turned off, and the jumper should be returned to the 4-5 position to restore normal operation. Default is for this jumper to be on pins 4-5.

Caution: This procedure should only be done if, after a BIOS update, the system does not boot to a point where BIOS Setup can be entered or if, after CMOS default settings have been restored from within the Setup program, the system does not boot to the operating system.

3. Revision of Peripheral Component Interconnect (PCI) PCIset Section

The fourth bullet in the first column in this section will be replaced in its entirety as follows:

- Fully synchronous PCI bus interface
    - — 25/30/33 MHz
    - — PCI to DRAM data transfers up to or greater than 100 MB/sec
    - — PCI to DRAM posting of 12 Dwords
    - — 5 Dword buffers for CPU to PCI write posting
    - — 4 Dword buffers for PCI to Memory bus master cycles
    - — Support for up to 5 PCI masters