Chapter 2

HARDWARE INSTALLATION

It is important to set jumpers correctly. Improper setting will cause system instability, destruction of components, and/or system hang-up

System Speed Selection: SW

The system board have reserved all possible core/bus ratio. Please see as below **figure** 2-1 and **table** 2-1.

Figure 2-1

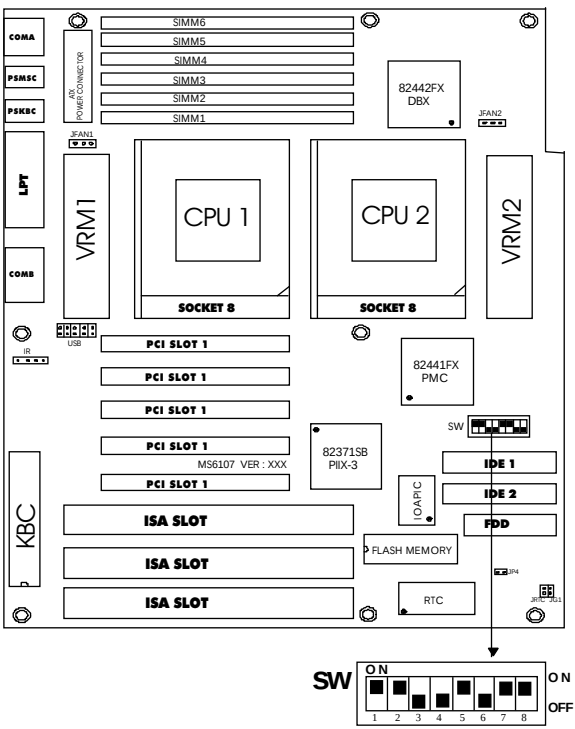
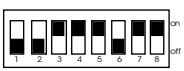


Table 2-1

CPU SPEED	SW SETTING	REMARK
150 MHZ		BUS CLOCK = 60MHZ CORE/BUS RATIO = 2.5
167 MHZ		BUS CLOCK = 66.6MHZ CORE/BUS RATIO = 2.5
180 MHZ		BUS CLOCK = 60MHZ CORE/BUS RATIO = 3
200 MHZ		BUS CLOCK = 66.6MHZ CORE/BUS RATIO = 3
233 MHZ		BUS CLOCK = 66.6MHZ CORE/BUS RATIO = 3.5

CMOS RAM CLEAR: JRTC

The system board configuration is stored in RTC's CMOS RAM. If you need to clear the system board configuration the process depends on whether or not the RTC type can be cleared or not. If the RTC is clearable then do the following:

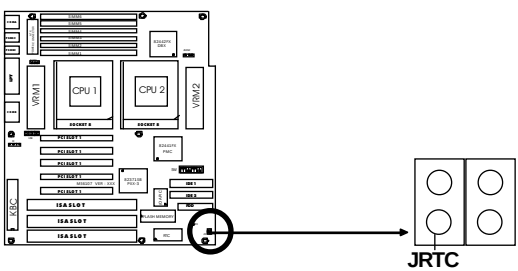
1. DALLAS's DS12887A-----Clear RTC while power is off.
    a. Turn power off.
    b. Short jumper JRTC.
    c. Turn power on.
    d. Enter the BIOS setup program to re-set up th system configuration.
    e. Reboot the system.

Note: *DALLAS DS12887 has no function for clearing.*

2. BENCHMARQ's BQ3287AMT-----Clear RTC while power is on.

    a. Turn power on.
    b. Short jumper JRTC, then open it.
    c. Reset the system by:
        - Turn off power then on.
        - Warm reset (PRESS Ctrl + Alt + Delete).
        - Use the reset button.
    d. Enter the BIOS setup program to reset the system configuration.
    e. Reboot the system.

Note: *BENCHMARQ's BQ3287 has no function for clearing.*



DRAM Population Rules

In order to create a memory array, certain rules must be followed.
The following set of rules allows optimum configuration.

1. DRAM modules must be populated in pairs; the memory array is 64 or 72 bits wide.
2. DRAM modules can be populated in any order(i.e. SIMM1/2 does not have to be populated before SIMM 3/4 are used).
3. DRAM modules pairs need to be populated with the same densities(single or double). For example, SIMM1/2 sockets must be populated with identical densities, but SIMM3/4 and SIMM5/6 sockets can be populated with different densities. In addition Asymmetric DRAMs of the same type should be used in a whole row.
4. BEDO, EDO, FP modes can be mixed in the memory array, but only one type should be used per SIMM socket pair. For example SIMM1/2 sockets can be populated with EDO while SIMM3/4 can be populated with FP mode type DRAM.
5. DRAM timing which provides the DRAM speed grade control for the entire memory array must be programmed to use the timing of the slowest DRAM that is currently installed.

Note: *1. Before using DRAM modules, make sure that the modules used is the same as in the chart next page.*
2. To use the ECC(Error Code Correct) function, a SIMM module with parity support must be used. You can turn on the ECC function in the BIOS setup

CHAPTER 2 HARDWARE INSTALLATION

System Memory Installation: SIMM6-SIMM1

To ease the user's difficulty, we're going to explain about the 72 pin SIMM DRAM Module. If the user's already familiar with this, you could skip this section. The 72 pin SIMM DRAM module are divided into two: single density and double density, each side may have 32-bits data and/or 4 parity bits(depends on what parity you have). Nowadays, DRAM Vendor only market 256Kbit, 1Mbit, 4Mbit, 8Mbit, 16Mbit and 64 Mbit DRAM chip with different density(256Kb and 1Mb are already very scarce in the market). DRAM chip with the same density may have different memory bank configuration. Lets take the density of 16Mbit may be 16MX1, 4MX4, 2MX8 or 1MX16. Please refer to the next page for the DRAM chip density, organization and SIMM module oraganization.

Fig. 2-2 DRAM Chip Density & Organization

DRAM chip density	Organization (words X bits)	Address Mode			refresh cycle	440 FX supports
		mode	# of row address	# of column address		
4Mb	1MX4	SYMM	10	10	1024	YES
	4MX1	SYMM	11	11	1024	YES
16Mb	16MX1	SYMM	12	12	4096	YES
	4MX4	SYMM	11	11	2048	YES
	2MX8	ASYMM	11	11	2048	YES
	1MX16	ASYMM	10	10	1024	YES
64Mb	16MX4	ASYMM	13	11	4096	NO
		SYMM	12	12	4096	YES
	8MX8	ASYMM	13	10	4096	NO
		ASYMM	12	11	4096	YES

Note: **SYMM** = symmetric **ASYMM** = asymmetric
If the Row address of the DRAM Chips equals the Column address then it's in the symmetric mode, otherwise it's in the asymmetric mode.

Fig. 2-3 72 Pin SIMM Module Density & Memory Size

Data DRAM Chip Density		Parity DRAM Chip Density	Module Organization				MB/SIMM	
			Single Side		Double Side			
			# of Data DRAM Chip	# of Parity DRAMChip (if have)	# of Data DRAM Chip	# of Parity DRAMChip (if have)	Single Side (S)	Double Side (D)
4Mb	1MX4	1MX1	8	4	16	8	4MB	8MB
	4MX1	4MX1	32	4	64	8	16MB	32MB
16Mb	16MX1	16MX1	32	4	64	8	64MB	128MB
	4MX4	4MX1	8	4	16	8	16MB	32MB
	2MX8	-	4	-	8	-	8MB	16MB
	1MX16	1MX1	2	4	4	8	4MB	8MB
64Mb	16MX4	16MX1	8	4	16	8	64MB	128MB

Note: **b** = bit **B** = byte

CHAPTER 2 HARDWARE INSTALLATION

DRAM Memory Installation

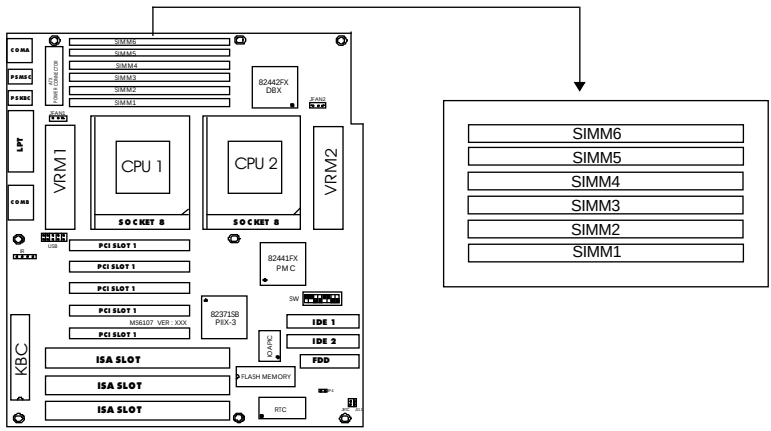


Table 2-4

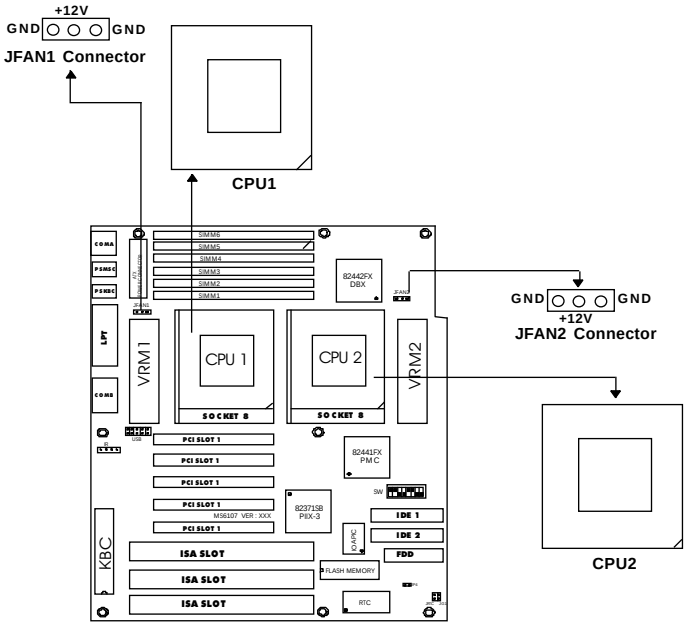
SIMM6	SIMM5	SIMM4	SIMM3	SIMM2	SIMM1
-	-	-	-	D/S	D/S
-	-	D/S	D/S	D/S	D/S
D/S	D/S	D/S	D/S	D/S	D/S
D/S	D/S	-	-	-	-
D/S	D/S	D/S	D/S	-	-

Module Population Rules

CHAPTER 2 HARDWARE INSTALLATION

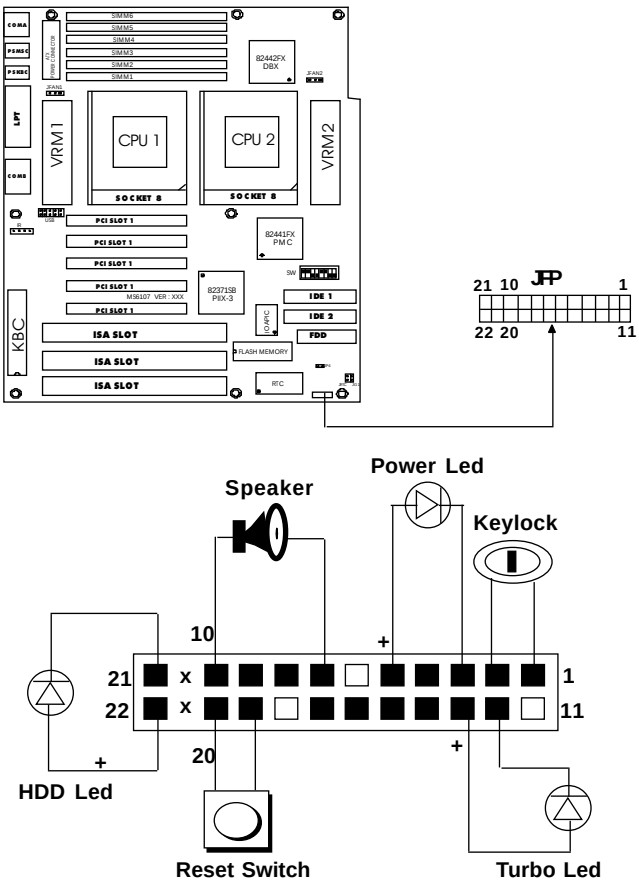
CPU Installation & Fan Power Connector: JFAN1, JFAN2

Open Socket 8 by pulling the lever away from the socket then upwards at a 90 degree right angle. Insert the CPU according to the orientation as shown. If it does not fit in easily, then try to move it in different direction, because the CPU pin configuration only fits one way as opposed to earlier CPUs. Make sure that the CPU is well seated, then close the lever. See the figure below:



Case Block Connector: JFP

The Turbo LED, Turbo switch, Hardware Reset, Key lock, Power LED, Speaker and HDD LED are all connected to the JFP connector block as shown below;

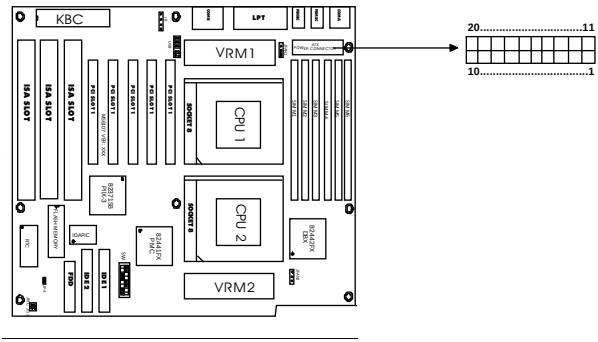


Note: *The hardware Turbo switch is non-functional, but it could be controlled by software Turbo/Deturbo*

CHAPTER 2 HARDWARE INSTALLATION

Power Supply Connector: PWR20

The power supply connector is a 20-pin ATX power connector. Connectors from the power supply can fit only in one direction as shown in the diagram below:

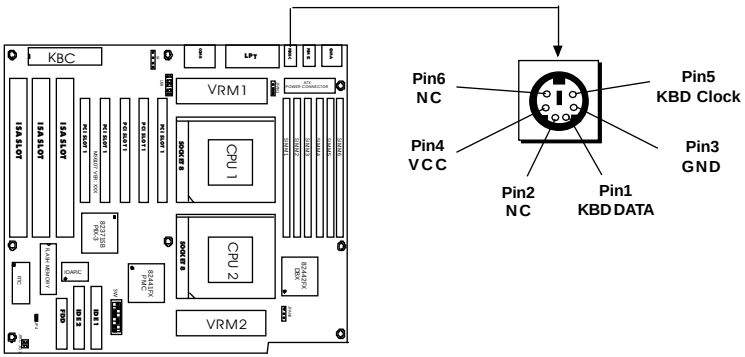


ATX Power Connector Pin Description

20	19	18	17	16	15	14	13	12	11
5V	5V	-5V	GND	GND	GND	PS_ON	GND	-12V	3.3V
12V	5V_SB	PW_Ok	GND	5V	GND	5V	GND	3.3V	3.3V
10	9	8	7	6	5	4	3	2	1

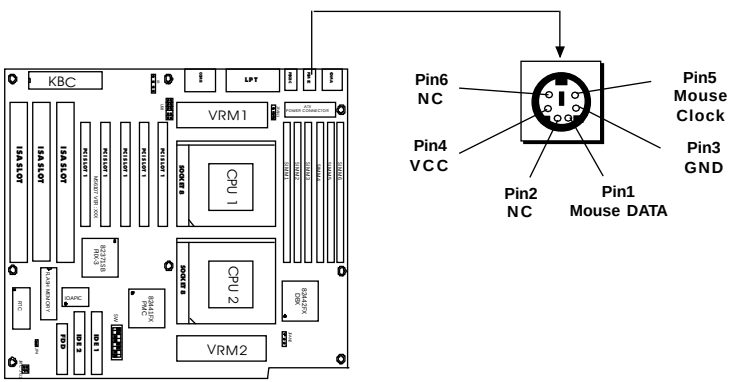
Keyboard Connector: PSKBC

The system board provides a standard PS/2 style keyboard mini DIN connector for attaching a keyboard. You can plug a keyboard cable directly to this connector.



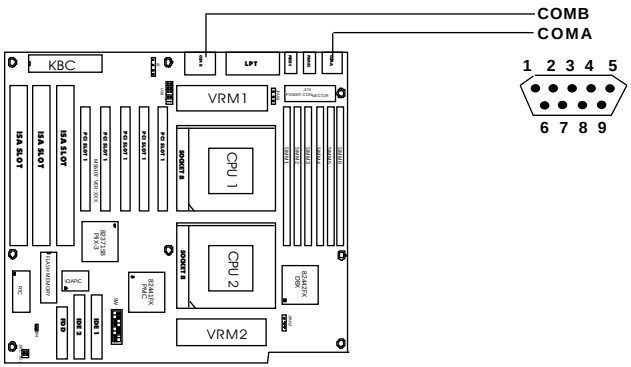
Mouse Connector: PSMSC

The system board provides a standard PS/2 style mouse mini DIN connector for attaching a PS/2 style mouse. You can plug a PS/2 style mouse directly into this connector. The connector location and pin definition as shown below:



Serial Port Connectors: COMA & COMB

The system board has two 9-pin male DIN connectors for serial ports COMA and COMB. These two ports are 16550A high speed communication ports that send/receive 16 bytes FIFOs. You can attach a mouse or a modem cable directly into these connectors.

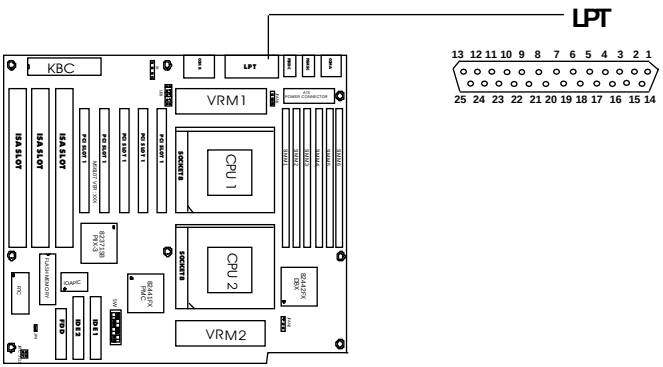


PIN DEFINITION

Pin #	Definition
1	**DCD**(Data Carry Detect)
2	**SIN**(Serial In or Receive Data)
3	**SOUT**(Serial Out or Transmit Data)
4	**DTR**(Data Terminal Ready)
5	**GND**
6	**DSR**(Data Set Ready)
7	**RTS**(Request To Send)
8	**CTS**(Clear To Send)
9	**RI**(Ring Indicate)

Parallel Port Connectors: LPT

The system board provides a 25 pin female centronic connector for LPT. A parallel port is a standard printer port that also supports Enhanced Parallel Port(EPP) and Extended capabilities Parallel Port(ECP). See connector and pin definition below:



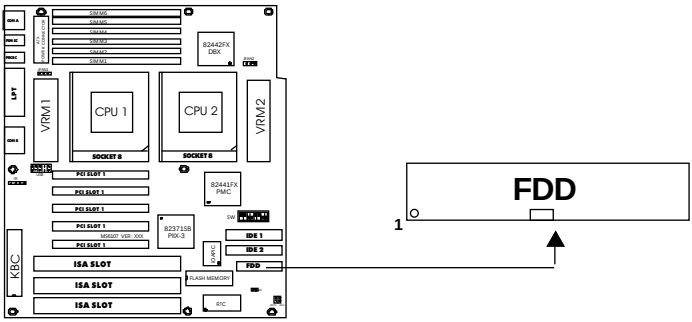
PIN DEFINITION

PIN #	DEFINITION	PIN #	DEFINITION
1	STROBE	14	AUTO FEED#
2	DATA0	15	ERR#
3	DATA1	16	INIT#
4	DATA2	17	SLIN#
5	DATA3	18	GND
6	DATA4	19	GND
7	DATA5	20	GND
8	DATA6	21	GND
9	DATA7	22	GND
10	ACK#	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SELECT		

CHAPTER 2 HARDWARE INSTALLATION

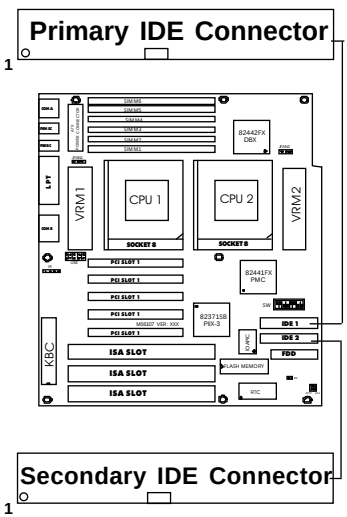
Floppy Disk Connector: FDD

The system board also provides a standard floppy disk connector FDD that supports 360K, 720K, 1.2M, 1.44M and 2.88M floppy disk types. You can attach a floppy disk cable directly to this connector.



Hard Disk Connector: IDE1 & IDE2

The system board has a 32-bit Enhanced PCI IDE Controller that provides for two HDD connectors IDE1(primary) and IDE2(secondary). You can connect up to four hard disk drives or other devices to IDE1 and IDE2.



IDE1(primary IDE connector)

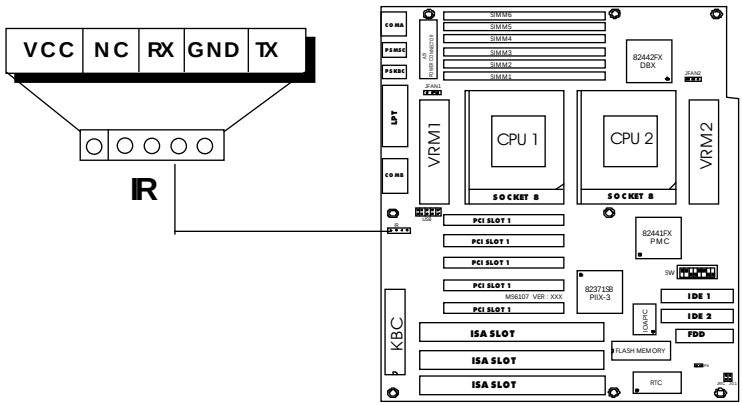
The first hard disk should always be connected to IDE1. IDE1 can connect a Master and a Slave drive.

IDE2(secondary IDE connector)

IDE2 can connect a Master and a Slave drive.

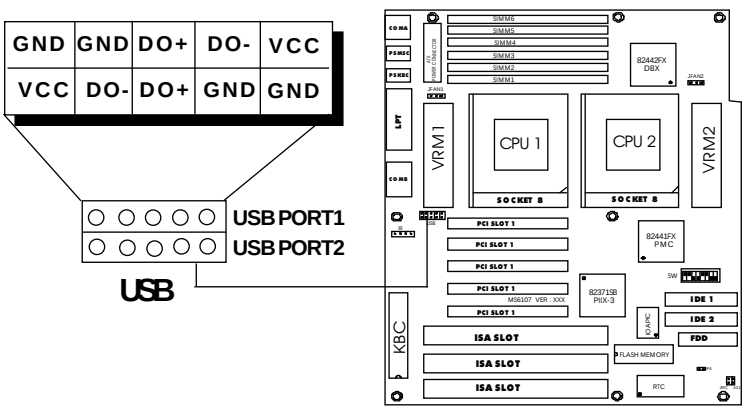
IrDA Infrared Module Connector: IR

The system board provides a 5-pin infrared connector(IR) for IR module.



USB Connector: USB

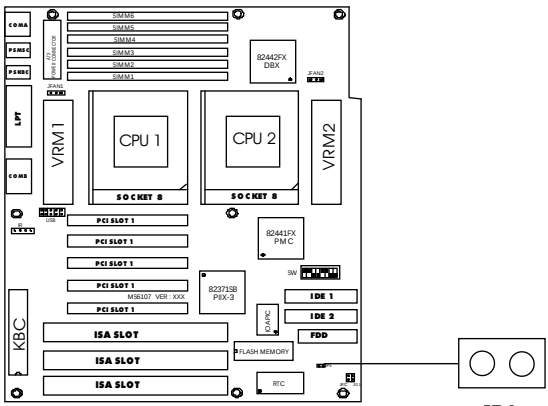
This 10-pin connector supports USB devices.



CHAPTER 2 HARDWARE INSTALLATION

Power Switch: JP4

The 2 -pin connector must utilize a toggle swtich (one push on/ second push off).



Power Saving Switch: JG1

Attaching a power saving switch to this connector will allow the system into sleep mode whenever the switch is pressed.