SUPER®

SUPER P6SLA
SUPER P6SLE

USER'S and BIOS MANUAL

Revision 1.3

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Preface

About This Manual

This manual is written for system houses, PC technicians and knowledgeable PC end users. It provides information for the installation and use of the SUPER P6SLA/P6SLE motherboard. SUPER P6SLA/P6SLE supports Pentium II 233/266/300/333 MHz.

The Pentium II processor with the Dual Independent Bus Architecture is housed in a new package technology called the Single Edge Contact (S.E.C.) cartridge. This new cartridge package and its associated "Slot 1" infrastructure will provide the headroom for future high-performance processors.

Manual Organization

Chapter 1, Introduction, describes the features, specifications and performance of the SUPER P6SLA/P6SLE system board, provides detailed information about the chipset, and offers warranty information.

Refer to Chapter 2, Installation, for instructions on how to install the Pentium II processor, the retention mechanism, and the heat sink support. This chapter provides you with instructions for handling static-sensitive devices. Read this chapter when you want to install or remove DIMM memory modules and to mount the system board in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, IDE interfaces, parallel port, serial ports, as well as the cables for the power supply, reset cable, Keylock/Power LED, speaker and keyboard.

If you encounter any problem, please see Chapter 3, Troubleshooting, which describes troubleshooting procedures for video, memory, and the setup configuration stored in memory. Instructions are also included on contacting a technical assistance support representative, returning merchandise for service and the BBS# for BIOS upgrades.

See Chapter 4 for configuration data and BIOS features.

Chapter 5 has information on running setup and includes default settings for Standard Setup, Advanced Setup, Chipset Function, Power Management, PCI/PnP Setup and Peripheral Setup.

Appendix A offers information on BIOS error beep codes.

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Chapter 1
Introduction

1-1 Overview

SUPER P6SLA/P6SLE supports single Pentium II. They are based on Intel's 440 LX chipset which enables Accelerated Graphics Port (AGP), Wake-on-LAN™, SDRAM, concurrent PCI and Ultra DMA 33 MB/s burst data transfer rate.

SUPER P6SLA/P6SLE is ATX size and have 4 PCI slots, 3 ISA slots and an AGP connector. These motherboards accommodate a total of 768 MB EDO or 384 MB SDRAM memory with 3 168-pin DIMM sockets.

AGP reduces contention with the CPU and I/O devices by broadening the bandwidth of graphics to memory. It delivers a maximum of 532 MB/s 2x transfer mode which is quadruple the PCI speed!

Wake-on-LAN allows remote network management and configuration of the PC, even in off-hours when the PC is turned off. This reduces the complexity of managing the network.

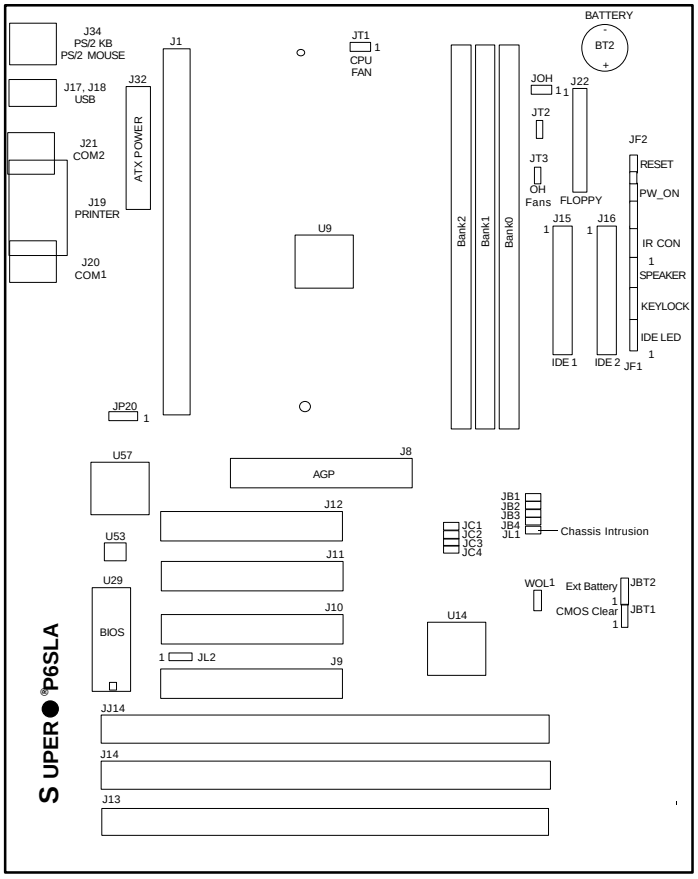
Other features that maximize customer satisfaction and simplicity in managing the computer are PC 98-ready and support for Advanced Configuration and Power Interface (ACPI). With PC Health Monitoring, you can protect your system from problems before they even occur.

Included I/O on Super P6SLA/P6SLE are 2 EIDE ports, a floppy port, an ECP/EPP parallel port, PS/2 mouse and PS/2 keyboard, 2 serial ports, an infrared port and 2 USB ports.

SUPER P6SLA

Figure 1-1. SUPER P6SLA Motherboard Picture

Figure 1-2. SUPER P6SLA Motherboard Layout



——— Manufacturer Settings ———

JL1: OFF (normal)
ON (intrusion)
JL2: OFF
JP20: 1-2 PIIX4 CTL
2-3 Save PD State (default)
JBT1: 1-2 (default)
2-3 CMOS Clear
To clear the CMOS completely, disconnect the power source.
WOL: Wake-on-LAN
JT1: CPU fan 1
JT2: CPU fan 2
JT3: Overheat fan

———————————————

CPU Core/ Bus Ratio	JB1	JB2	JB3	JB4
3.0	ON	OFF	ON	ON
3.5	OFF	OFF	ON	ON
4.0	ON	ON	OFF	ON
4.5	OFF	ON	OFF	ON
5.0	ON	OFF	OFF	ON

———Bus Speed———

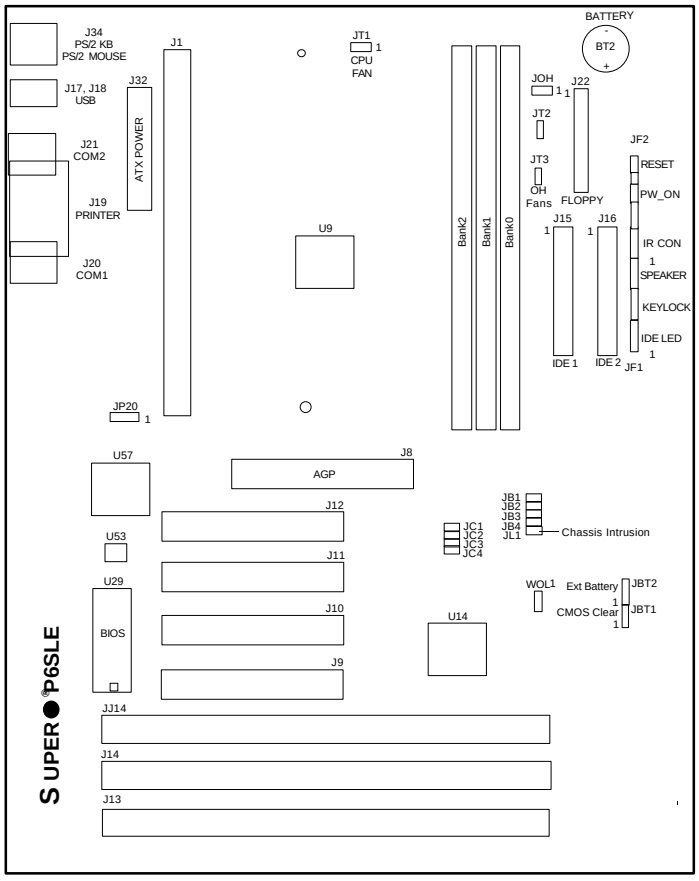
MHz	JC1	JC2	JC3
50	ON	ON	ON
60	ON	OFF	OFF
66	OFF	OFF	OFF (default)
75	OFF	ON	OFF

———————————————

SUPER P6SLE

Figure 1-3. SUPER P6SLE Motherboard Picture

Figure 1-4. SUPER P6SLE Motherboard Layout



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5.0	ON	OFF	OFF	ON

———Bus Speed———

MHz	JC1	JC2	JC3
50	ON	ON	ON
60	ON	OFF	OFF
66	OFF	OFF	OFF (default)
75	OFF	ON	OFF

———————————————

SUPER P6SLA Features

The following list covers the general features of SUPER P6SLA:

CPU
- Single Pentium II processor 233/266/300/333 MHz

Memory
- 768 MB EDO or 384 MB SDRAM
- Error Checking and Correction and Parity Checking support

Chipset
- Intel 440LX

Expansion Slots
- 4 PCI slots
- 3 ISA slots
- 1 AGP slot

BIOS
- AMI® Flash WINBIOS with boot block support
- DMI 2.0, Plug and Play (PnP)

PC Health Monitoring (W83781D)
- Seven on-board voltage monitors for the CPU core, CPU I/O, +3.3V, ±5V, and ±12V
- Three-fan status monitors with firmware/software control on/off
- Environment temperature monitor and control
- CPU fan auto-off in sleep mode
- CPU overheat control and alarm
- Chassis intrusion detection
- System resource alert
- Hardware BIOS virus protection
- Switching voltage regulator for the CPU core
- SUPERMICRO SUPER Doctor and Intel LANDesk® Client Manager (LDCM) support

ACPI/PC 98 Features
- Microsoft® OnNow
- Slow blinking LED for suspend-state indicator
- BIOS support for USB keyboard
- Real time clock wake-up alarm
- Main switch override mechanism
- External modem ring-on

On-Board I/O

- 2 EIDE Bus Master interfaces support Ultra DMA/33 and PIO Mode 4
- 1 floppy interface
- 2 Fast UART 16550 serial ports
- EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port) parallel port
- PS/2 mouse and PS/2 keyboard
- Infrared port
- 2 USB ports

Dimensions

- ATX (12" x 7")

CD Utilities

- Intel LANDesk Client Manager for Windows NT® and Windows 95® (optional)
- PIIX4 Upgrade Utility for Windows 95
- BIOS Flash Upgrade Utility
- DMI Browser for Windows 95
- DMI Wizard
- Super Doctor Utility ver 1.21b

SUPER P6SLE Features

The following list covers the general features of SUPER P6SLE:

CPU
- Single Pentium II processor 233/266/300/333 MHz

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Chipset
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Mode 4

- 1 floppy interface
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- Super Doctor Utility ver 1.21b

1-2 PC Health Monitoring

This section describes the PC health monitoring features of SUPER P6SLA/P6SLE. It has an on-board W83781D System Hardware Monitor chip which can support PC health monitoring.

Seven On-Board Voltage Monitors for the CPU Core, CPU I/O, +3.3V, ±5V, and ±12V
The on-board voltage monitor will scan the seven monitored voltages every second. Once a voltage becomes unstable, it will report a warning or an error message on the screen. Users can adjust the threshold of the monitored voltage to determine the sensitivity of the voltage monitor.

Three-Fan Status Monitors with Firmware/Software Control On/ Off
The PC health monitor can check the RPM status of the cooling fans. The on-board 3-pin CPU fan is controlled by the ACPI BIOS and the ACPI enabled operating system. The thermal fans are controlled by the overheat detection logic.

Environment Temperature Control
The thermal control sensor will monitor the real-time environment temperature. It will turn on the back-up fan whenever the environment temperature goes over the user-defined threshold. The overheat circuitry runs independently from the CPU . It can still monitor the overheat condition even if the CPU is in sleep mode. Once it detects that the environment temperature is too high, it will automatically turn on the back-up fan to prevent any overheat damage to the CPU. The on-board chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

CPU Fan Auto-Off in Sleep Mode
The CPU fan will turn on when the power is on. It can be turned off when the CPU is in sleep mode. When the CPU is in sleep mode, it means that it will not run at full power, thereby generating less heat. For power saving purposes, the user can have the option to shut down the CPU fan.

CPU Overheat Alarm and Control
This feature is available when used with SUPERMICRO's SUPER Doctor Utility. The program will generate a beep sound via the

speaker when it detects a CPU overheat condition. This overheat condition can be configured by the user. The program can also give an indication on the screen when the CPU overheats.

Chassis Intrusion Detection
The chassis intrusion circuitry can detect unauthorized intrusion to the system. The chassis intrusion connector is located on JL1. Attach a micro-switch to JL1. When the micro-switch is closed, it means that the chassis has been opened. The circuitry will then alert the user with a warning message when the system is on. The circuitry uses the on-board battery to power up, so even if the whole system is powered off, the detection can still work properly.

System Resource Alert
This feature is available when used with Intel LANDesk Client Manager. The user can be notified of certain system events. For example, if the system is running low on virtual memory, the hard drive space is not enough to save the data, you are then alerted of the potential problems.

Hardware BIOS Virus Protection
The system BIOS is protected by hardware so that no virus can infect the BIOS area. The user can only change the BIOS content through the flash utility provided by SUPERMICRO. This feature prevents viruses from infecting the BIOS area and loss of valuable data. There is also a second way to protect the BIOS from infection. Please refer to section 5-2-2, Anti-Virus, on page 5-21.

Switching Voltage Regulator for the CPU Core
The switching voltage regulator for the CPU core can support up to 20A current, with auto-sensing voltage ID ranging from 1.3V to 3.5V. This allows the regulator to run cooler and makes the system more stable.

Intel LANDesk Client Manager (LDCM) Support
As the computer industry grows, PC systems become more complex and harder to manage. Historically, only experts could fully understand and control these complex systems. Today's users want manageable systems that interact automatically with the user. Client Manager enables both administrators and clients to:

- Review system inventory
- View DMI-compliant component information
- Back-up and restore system configuration files
- Troubleshoot
- Receive notification for system events
- Transfer files to and from client workstations
- Remotely reboot client workstations

1-3 ACPI/PC 98 Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives, and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, phones, and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 95 and Windows NT.

Microsoft OnNow
The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears off and responds immediately to user or other requests.

Slow Blinking LED for Sleep-state Indicator
When the CPU goes into a suspend state, the power LED will start blinking to indicate that the CPU is in sleep mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

BIOS Support for USB Keyboard
If the USB keyboard is the only keyboard in the system, the USB keyboard will work like a normal keyboard during system boot-up.

Real Time Clock Wake-up Alarm
The PC is perceived to be off when not in use, but is still capable of responding to previously scheduled wake-up events. The user can set up a timer to wake-up or shutdown the system at some predetermined date or time of the month.

Main Switch Override Mechanism
When an ATX power supply is used, the power button can function as a system suspend button. When the user presses on the power button, the system will enter a SoftOff state. The monitor will be suspended, and the hard drive will spin down. Pressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry on the system alive. In case the system malfunctions and you want to turn off the power, just press down on the power button for approximately 4 seconds. The power will turn off and no power is provided to the motherboard.

External Modem Ring-on
Wake-up events can be triggered by a device such as the external modem ringing when the system is in SoftOff state. When the modem rings, the system behaves as if a user pressed the PW_ON button.

1-4 Chipset Overview

The 440LX chipset was developed by Intel as the ultimate Pentium II processor platform targeted for emerging 3D graphics and multimedia applications. Along with System-to-PCI bridge integrated with optimized DRAM controller and data path, the chipset introduces the Accelerated Graphics Port (AGP) interface. AGP is a high performance, component level interconnect targeted at 3D applications and is based on a set of performance enhancements to PCI. The I/O subsystem portion of the 440LX platform is based on the PIIX4, a highly integrated version of Intel's PCI-to-ISA bridge family.

The 440LX PCI/AGP Controller (PAC) system bus interface supports up to two Pentium II processors. It provides an optimized 72-bit DRAM interface (64-bit data plus ECC). This interface supports 3.3V DRAM technologies. The PAC provides the inter-

face to a PCI bus operating at 33 MHz. This interface implementation is compliant with the PCI Rev 2.1 Specification. The AGP interface is based on the AGP Specification Rev 1.0. It can support up to 133 MHz (532 MB/s) data transfer rates.

1-5 Wake-On-LAN (WOL)

Wake-on-LAN is defined as the ability of a management application to remotely power up a computer which is powered off. Remote PC setup, updates, and asset tracking can occur after hours and on weekends so daily LAN traffic is kept to a minimum and users are not interrupted.

The motherboard has a 3-pin header (WOL) used to connect to the 3-pin header on the Network Interface Card (NIC) which has WOL capability.

1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for high CPU clock rates like 333, 300, 266, 233 MHz Pentium II processors.

SUPER P6SLA/P6SLE accommodates ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some power supplies are not adequate.

It is highly recommended that you use a high quality power supply. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to separate noise from the computer. You can also install a power surge protector to help avoid problems caused by power surges.

1-7 Super I/O

The disk drive adapter functions of Super I/O chip W83977TF (P6SLA) / SMCW602 (P6SLE) include a floppy disk drive controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the Super

I/O greatly reduced the number of components required for interfacing with floppy disk drives. The Super I/O supports two 360 K, 720 K, 1.2 M, 1.44 M, or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s.

The Super I/O provides two high speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2 Kbps and also advanced speed with baud rates of 230 K, 460 K, or 921 Kbps which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Also available, through the printer port interface pins, are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface). It also has auto power management to reduce power consumption.

The Super I/O complies with **Microsoft PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resources are flexible to adjust to meet ISA PnP requirement. Moreover, it meets the specification of PC97's requirement in the power management: ACPI and DPM (Device Power Management).

1-8 Warranty, Technical Support, and Service

The manufacturer will repair or exchange any unit or parts free of charge due to manufacturing defects for one year (12 months) from the original invoice date of purchase.

Parts

Defective parts will be exchanged or repaired within one year (12 months) from the manufacturer’s original invoice purchase date.

BIOS
The manufacturer will exchange the BIOS (shipping and handling excluded) due to existing incompatibility issues within one year from the manufacturer's original invoice purchase date.

Labor
Mail-in or carry-in service is available for one year (12 months) from the manufacturer's original invoice purchase date.

Returns
If you must return products for any reason, refer to Chapter 3 in this manual, "Returning Merchandise for Service."

Chapter 2
Installation

2-1 Static-Sensitive Devices

Static-sensitive electric discharge can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge.

Precautions

- Use a grounded wrist strap designed for static discharge.
- Touch a grounded metal object before you remove the board from the anti-static bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules, or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the system board and peripherals back into their anti-static bags when not in use.
- For grounding purposes, be sure your computer system's chassis allows excellent conductive contacts between its power supply, case, mounting fasteners, and the system board.

Unpacking

The system board is shipped in anti-static packaging to avoid static damage. When unpacking the board, be sure the person handling the board is static-protected.

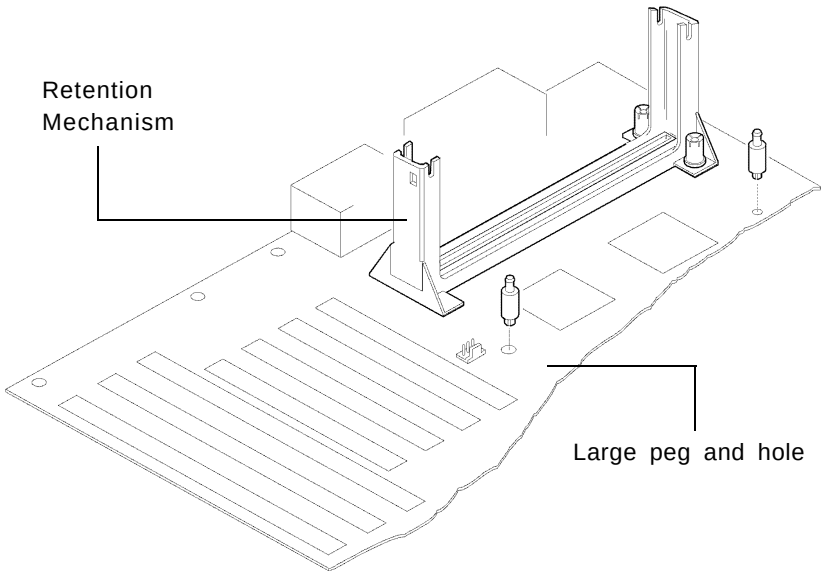
2-2 Pentium II Processor Installation

When handling the Pentium II processor, avoid placing direct pressure on the label area of the fan.

1. Check the Intel boxed processor kit for the following items: the processor with the fan heatsink attached, two black plastic pegs, two black plastic supports, and one power cable.

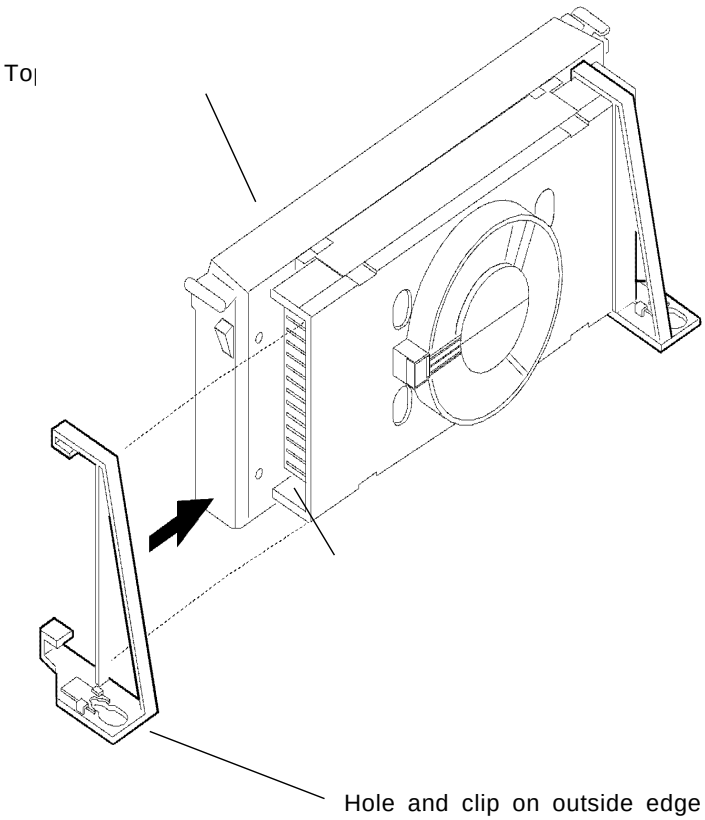
2. Install the retention mechanism attach mount under the motherboard, before mounting the motherboard into the chassis. Do not screw too tightly. Mount the two black plastic pegs onto the motherboard (Figure 2.1). These pegs will be used to attach the fan heatsink supports. Notice that one hole and the base of one peg are larger than the other hole and peg base. Push each peg into its hole firmly until you hear it "click" into place.

Figure 2-1. Mounting the Pegs



3. Slide a black plastic support onto each end of the fan heatsink, making sure that the hole and clip are on the outside edge of the support. If the supports are reversed, the holes will not line up with the pegs on the motherboard. Slide each support toward the center of the processor until the support is seated in the outside groove in the fan housing.

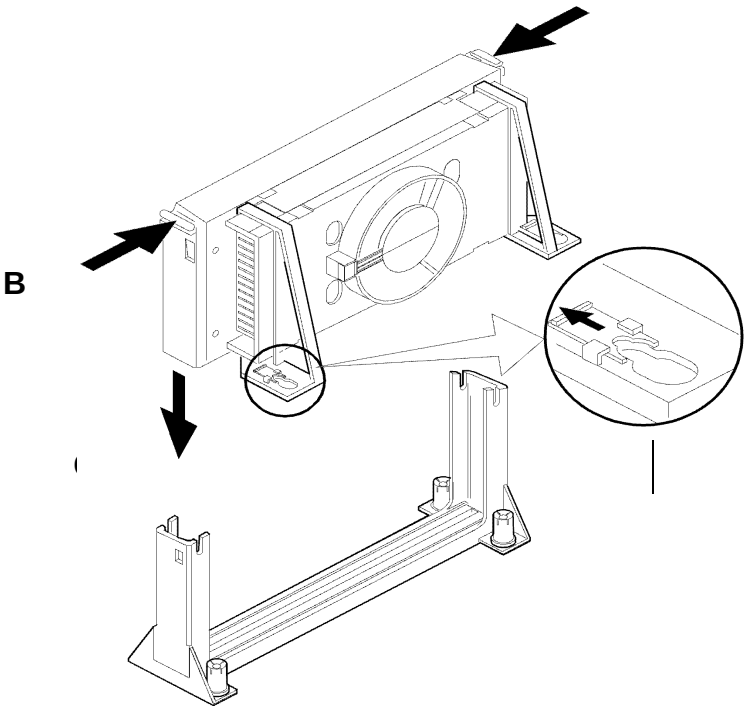
Figure 2-2. Support for Fan Heatsink



4. Slide the clip (A) on each support toward the processor, exposing the hole that will fit over the peg on the motherboard. Push the latches (B) on the processor toward the center of the processor until they click into place.

5. Hold the processor so that the fan shroud is facing toward the pegs on the motherboard. Slide the processor (C) into the retention mechanism and slide the supports onto the pegs. Ensure that the pegs on the motherboard slide into the holes in the heatsink support and that the alignment notch in the SEC cartridge fits over the plug in Slot 1. Push the processor down firmly, with even pressure on both sides of the top, until it is seated.

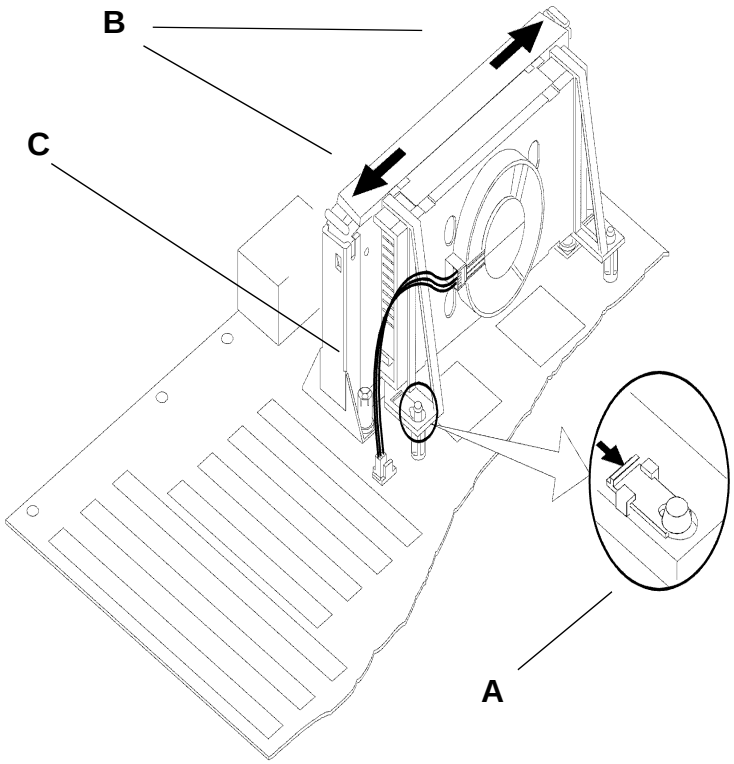
Figure 2-3. Retention Mechanism



6. Slide the clips on the supports (A) forward until they click into place to hold the pegs securely. Apply slight pressure on the peg and push the peg toward the clip while pushing the clip forward. Push the latches on the processor (B) outward until they click into place in the retention mechanism. The latches must be secured for proper electrical connection of the processor.

7. Attach the small end of the power cable (C) to the three-pin connector on the processor, then attach the large end to the three-pin connector on the motherboard.

Figure 2-4. Attaching the Power Cable



OEM Pentium II and Heat Sink Support

The heat sink support shown on Figure 2-5 consists of a top bar and a base bar with four posts on the top bar and two posts on the base bar. The two posts on the base snap into the motherboard. Install the two pins into the base bar. Insert the Pentium II with the heat sink on it into Slot 1. Install the top support bar. The four top posts should be close to Slot 1. The bottommost row of fins in the heat sink should fit between the top support bar and the bottom support bar as shown in Figure 2-6.

Figure 2-5. Heat Sink Support

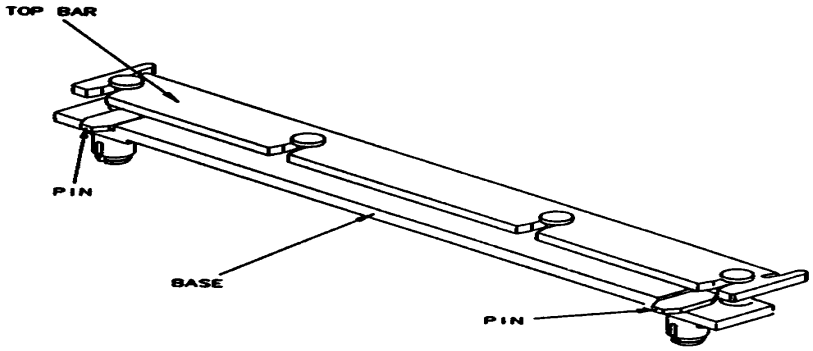
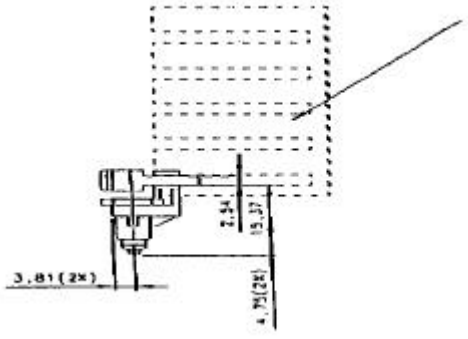


Figure 2-6. Pentium II Heat Sink



Removing the Pentium II Processor

When removing the Pentium II processor, avoid pressing down on the motherboard or components. Instead, press down on the plastic connectors.

To remove the Pentium II processor from the motherboard, follow these steps (the reverse of the installation process).

1. Disconnect the fan power cable from the motherboard. It is recommended to leave the cable connected to the processor.

2. Slide the clips on the supports backward to release the pegs in the motherboard. Push the latches on the processor toward the center of the processor until they click into place.

3. Lift one end of the processor until it is freed from Slot 1. Lift the other end of the processor until it is freed from Slot 1. Lift the entire processor (with the fan heatsink supports attached) until it is free from the retention mechanism.

4. Remove the heatsink support pegs from the motherboard and discard them. With one hand, squeeze together the two halves of the peg on the bottom side of the motherboard. With the other hand, pull the peg out of the hole in the motherboard. Do not reuse the pegs.

2-3 Changing the CPU Speed

To change the CPU speed for a Pentium II processor, change the jumpers shown below on Table 2-1. Refer to Table 2-2 for the external bus speed jumper settings. The default bus speed is 66 MHz. The following example will show you which CPU Core/Bus Ratio to use. The general rule is to divide the CPU speed by the bus speed (66 MHz). If you have a 266 MHz CPU, dividing it by 66 will give you a CPU Core/Bus Ratio of 4. After determining the CPU Core/Bus Ratio, refer to Table 2-1 for settings of JB1, JB2, JB3 and JB4.

$$\text{CPU Core/Bus Ratio} = \frac{\text{CPU Speed}}{\text{Bus Frequency}}$$

$$\text{CPU Core/Bus Ratio} = \frac{266\ \text{MHz}}{66\ \text{MHz}} = 4.0$$

Table 2-1. Pentium II Speed Selection

CPU Core/ Bus Ratio	JB1	JB2	JB3	JB4
3.0	ON	OFF	ON	ON
3.5	OFF	OFF	ON	ON
4.0	ON	ON	OFF	ON
4.5	OFF	ON	OFF	ON
5.0	ON	OFF	OFF	ON

Table 2-2. External Bus Speed Selection

MHz	JC1	JC2	JC3
50	ON	ON	ON
60	ON	OFF	OFF
66	OFF	OFF	OFF
75	OFF	ON	OFF

Turbo Function
There are no jumpers for turbo switch and turbo LED. By default, the motherboard is running in full speed.

2-4 Mounting the Motherboard in the Chassis

The motherboard has standard mounting holes to fit different types of chassis. Chassis may come with a variety of mounting fasteners, made of metal or plastic. Although a chassis may have both metal and plastic fasteners, metal fasteners are the most highly recommended because they ground the system board to the chassis. Therefore, use as many metal fasteners as possible for better grounding.

2-5 Connecting Cables

Power Supply Connector
After you have securely mounted the motherboard to the chassis, you are ready to connect the cables. Attach power supply cable to J32 for an ATX power supply. See Table 2-3 for pin definitions of an ATX power supply.

Table 2-3. ATX Power Supply Connector Pin Definitions

Connector Number	Pin Number	Function	Pin Number	Function
J32	1	3.3V	11	3.3V
	2	3.3V	12	-12V
	3	COM	13	COM
	4	5V	14	PS-ON
	5	COM	15	COM
	6	5V	16	COM
	7	COM	17	COM
	8	PW-OK	18	-5V
	9	5VSB	19	5V
	10	12V	20	5V

PW_ON Connector

The PW_ON connector is located on pins 9 and 10 of JF2. Momentarily contacting both pins will power on/off the system. To turn off the power, hold down the power button for at least 4 seconds. The user can also configure this button as an on/off switch in the BIOS setup menu. See Table 2-4 for pin definitions.

Table 2-4. PW_ON Connector Pin Definitions

Pin Number	Definition
9	PW_ON
10	Ground

Infrared Connector

The infrared connector is located on pins 1-8 of JF2. See Table 2-5 for pin definitions.

Table 2-5. Infrared Pin Definitions

Pin Number	Definition
1	+5V
2	Key
3	IRRX
4	Ground
5	IRTX
6	IRSEL0
7	IRSEL1
8	IRSEL2

Reset Connector

The reset connector is located on pins 12 and 13 of JF2. This connector attaches to the hardware Reset switch on the computer case. See Table 2-6 for pin definitions.

Table 2-6. Reset Pin Definitions

Pin Number	Definition
12	Reset
13	Ground

Keylock/Power LED Connector

The keylock/power LED connector is located on pins 5 to 9 of JF1. See Table 2-7 for pin definitions. Pins 5 and 7 are for the power LED. Pins 8 and 9 are for the keylock.

Table 2-7. Keylock/Power LED Pin Definitions

Pin Number	Function	Definition
5	VCC (+5v)	Red wire, LED power
6	Key	No connection
7	GND	Black wire
8		Keyboard inhibit
9	GND	Black wire

Hard Drive LED

The hard drive LED is located on pins 1 to 4 of JF1. Attach the hard drive LED cable onto pins 1 and 2. See Table 2-8 for pin definitions.

Table 2-8. Hard Drive LED Pin Definitions

Pin Number	Definition
1	+5V
2	Key
3	HD Active
4	+5V

Speaker Connector
The speaker connector is located on pins 10 to 13 of JF1. See Table 2-9 for pin definitions.

Table 2-9. Speaker Connector Pin Definitions

Pin Number	Function	Definition
10	+	Red wire, speaker data
11	Key	No connection
12	VCC	Speaker data
13	GND	Black wire

Power Save State Select
Refer to Table 2-10 on how to set JP20. Power Save State Select is used when you want the system to be in power off state the first time you apply power to the system or when the system comes back from AC power failure. In the Power Save State the power will not come on unless you hit the power switch on the motherboard. PIIX4 control is used if you want the system to be in power on state the first time you apply power to the system or when the system comes back from AC power failure.

Table 2-10. JP20 Pin Definitions

Connector Number	Jumper Position	Function
JP20	1-2	PIIX4 Ctrl
	2-3	Save PD State

Chassis Intrusion Detector
The Chassis Intrusion detector is located on JL1. See Table 2-11 for pin definitions.

Table 2-11. Chassis Intrusion Detector Settings

Jumper	Definition
OFF	Normal
ON	Intrusion

ATX PS/2 Keyboard and PS/2 Mouse Ports
The ATX PS/2 keyboard and the PS/2 mouse are located on J34. See Table 2-12 for pin definitions.

Table 2-12. PS/2 Keyboard and Mouse Pin Definitions

Pin Number	Function
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

Universal Serial Bus
Two Universal Serial Bus connectors are located on J17 and J18. See Table 2-13 for pin definitions.

Table 2-13. USB Pin Definitions

Pin Number	J17 Function	Pin Number	J18 Function
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	GND	4	GND
5	N/A	5	Key

ATX Serial Ports
ATX serial port COM1 is located on J20 and serial port COM2 is located on J21. See Table 2-14 for pin definitions.

Table 2-14. Serial Ports Pin Definitions

Pin Number	Function	Pin Number	Function
1	DCD	6	CTS
2	DSR	7	DTR
3	Serial In	8	RI
4	RTS	9	GND
5	Serial Out	10	NC

CMOS Clear

Refer to Table 2-15 on how to clear the CMOS. **For ATX power supply, you need to completely shut down the system, then use JBT1 to clear the CMOS.** Do not use the PW_ON connector to clear the CMOS. A second way of resetting the CMOS contents is by pressing the <ins> key, then turning on the system power. Release the key when the power comes on.

Table 2-15. CMOS Clear Pin Definitions

Connector Number	Jumper Position	Function
JBT1	1-2 2-3	Normal CMOS Clear

External Battery

Connect an external battery to JBT2. Refer to Table 2-16 for pin definitions.

Table 2-16. External Battery Pin Definitions

Pin Number	Function
1	+3 V
2	NC
3	NC
4	Ground

Wake-on-LAN

The Wake-on-LAN connector is located on WOL1. Refer to Table 2-17 for pin definitions.

Table 2-17. Wake-on-LAN Pin Definitions

Pin Number	Function
1	+5V Standby
2	Ground
3	Wake up

Fan Connectors*

The thermal/overheat fan is located on JT3. The CPU fans are located on JT1 and JT2. Refer to Table 2-18 for pin definitions.

Table 2-18. Fan Pin Definitions

Pin Number	Function
1	Ground
2	+12 V
3	Tachometer

Overheat LED

The Overheat LED is located on JOH. Refer to Table 2-19 for pin definitions.

Table 2-19. Overheat LED Pin Definitions

Pin Number	Function
1	+12 V
2	Signal

* Caution: These connectors are DC direct.

2-6 Installing/Removing the DIMM Modules

SUPER P6SLA/P6SLE can accommodate a maximum of 768 MB EDO or 384 MB SDRAM. Note: SDRAM requires a minimum of one bank.

There are three types of EDO and SDRAM DIMM modules: x4, x8 and x16. If you are using the x4 type, you can populate the DIMM slots with either 4 single-sided memory modules or 2 double-sided memory modules. For memory configurations of 512 MB EDO DIMMs or higher, it is recommended to use the x8 or x16 type of memory. It is not recommended to mix EDO DIMM modules with SDRAM DIMM modules.

There are no jumpers needed to configure the on-board memory. Memory timing requires 70ns or faster for EDO memory. Refer to Figure 2-7 and the instructions below for installing or removing DIMM modules.

CAUTION

Exercise extreme care when installing or removing the DIMM modules to prevent any possible damage.

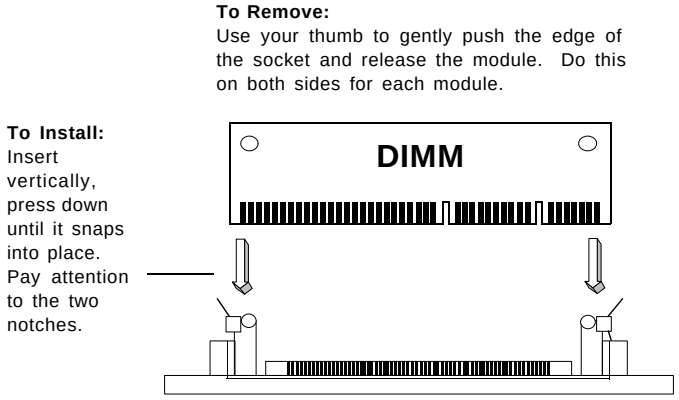
DIMM Module Installation

1. Insert DIMM modules in Bank 0 through Bank 2 as required for the desired system memory.
2. Insert each DIMM module vertically into its socket. Pay attention to the two notches to prevent inserting the DIMM at a wrong position. The component side of the DIMM module must face the CPU socket. The latter statement is applicable for DIMMs with components on one side only.
3. Gently press the DIMM module until it snaps upright into place in the socket.

Removing DIMM Modules

1. Remove DIMM modules in any order.
2. Gently push the edge of the sockets to the side to release the module. Remove one side of the DIMM module first, and then the other side, to prevent breaking the socket.

Figure 2-7. Installing/Removing a DIMM Memory Module



2-7 Connecting Parallel, Floppy and Hard Disk Drives

Use the following information to connect the floppy and hard disk drive cables.

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have the twisted wires always connects to drive B.
- An IDE hard disk drive requires a data ribbon cable with 40 wires, and a SCSI hard disk drive requires a SCSI ribbon cable with 50 wires. A wide SCSI hard disk drive requires a SCSI ribbon cable with 68 wires.
- A single IDE hard disk drive cable has two connectors to provide for two drives. To select an IDE disk drive as C, you would normally set the drive select jumper on the drive to DS1 (or Master). To select an IDE disk drive as D, you would normally set the drive select jumper on the drive to DS2 (or Slave). Consult the documentation that came with your disk drive for details on actual jumper locations and settings.
- A single SCSI ribbon cable typically has three connectors to provide for two hard disk drives and the SCSI adapter. (Note:

most SCSI hard drives are single-ended SCSI devices.) The SCSI ID is determined by jumpers or a switch on the SCSI device. The last internal (and external) SCSI device cabled to the SCSI adapter must be terminated.

- Some drives require a special controller card. Read your disk drive manual for details.

Parallel Port Connector

The parallel port is located on J19. See Table 2-20 for pin definitions.

Table 2-20. Parallel Port Pin Definitions

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK-	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

Floppy Connector

The floppy connector is located on J22. See Table 2-21 for pin definitions.

Table 2-21. Floppy Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

IDE Interfaces

There are no jumpers to configure the on-board IDE interfaces J15 and J16. Refer to Table 2-22 for the pin definitions.

Table 2-22. IDE Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

Chapter 3
Troubleshooting

3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

No Video

Use the following steps for troubleshooting your system configuration.

1. If you have no video, remove all the add-on cards and cables.
2. Check for shorted connections, especially under the motherboard.
3. Check the jumpers settings, clock speed, and voltage settings.
4. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details about beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended for port 80h codes. Refer to Appendix B.

Memory Error

If you encounter memory error, follow the procedures below.

1. Check to determine if DIMM modules are improperly installed.
2. Make sure that different types of DIMMs have not been installed in different banks (e.g., a mixture of 2MB x 36 and 1 MB x 36 DIMMs in Banks 0).
3. Determine if different speeds of DIMMs have been installed in the same or different banks, and the BIOS setup is configured

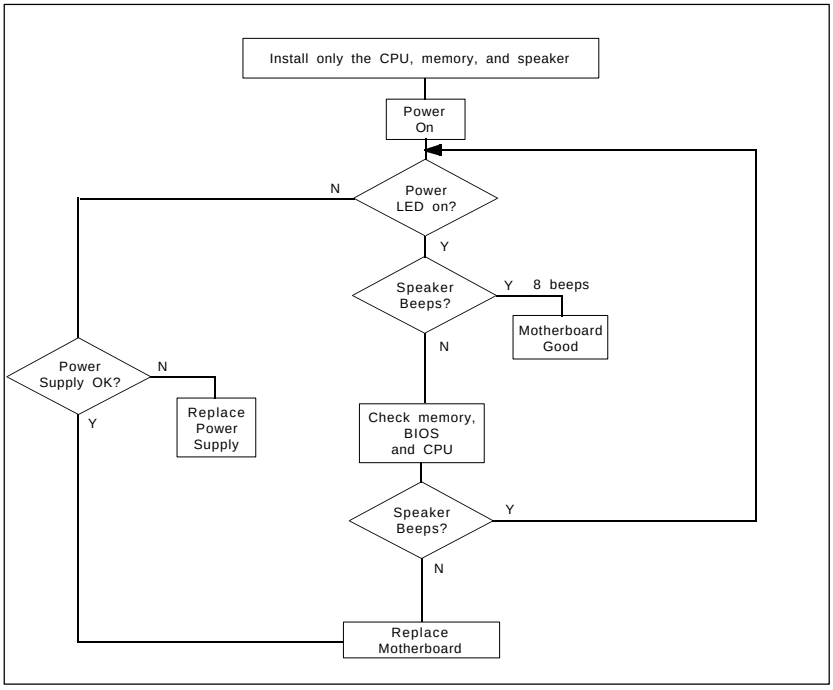


Figure 3-1. Troubleshooting Flowchart

for the fastest speed of RAM used. It is recommended to use the same RAM speed for DIMMs in different banks.

4. Check for bad DIMM modules or chips.

Losing the System's Setup Configuration

1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose CMOS setup. Refer to Chapter 1 of this manual for details.
2. If the above step does not fix the Setup Configuration problem, contact your vendor for repair.

3-2 Technical Support Procedures

1. Go through the 'Troubleshooting Procedures' section in this chapter of the manual before calling Technical Support.
2. Check FAQ on our web site at www.supermicro.com.

3. During the warranty period, contact your distributor first for any product problems.
4. BIOS upgrades can be downloaded from the SUPER BBS# (408) 895-2022, 24 hours a day, using 1200-14400 baud, 8 data bits, 1 stop bit and no parity. BIOS upgrades can also be downloaded from our web site at ftp://ftp.supermicro.com.

   Note: Not all BIOS can be flashed depending on the modifications on the boot block code.

5. If you still cannot get the problem resolved, have the following information ready before you call for technical support:

   - BIOS release date/version
   - System board serial number
   - Product model name
   - Invoice number and date
   - System configuration

3-3 Frequently Asked Questions

Question: **How do I update my BIOS?**
Answer: Update Bios files are located on our web site at www.supermicro.com. Please check the current BIOS revision and make sure it is more current than your BIOS. Select your motherboard model and the upgrade will be automatically selected and downloaded to your computer. Unzip the BIOS update file and you will find three files: readme.txt (flash instructions), sm2flash.com (BIOS flash utility), and the BIOS image file (xxxxxx.rom). Place these files on a bootable floppy and reboot your system. There are no BIOS boot block protection jumpers on the motherboard. At the BIOS prompt please enter the command "sm2flash." This will start the flash utility and give you an opportunity to first save your current file, flash the boot block and enter the name of the update BIOS image file. NOTE: It is very important that you save your current BIOS and name it "super.rom" in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select "Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS please clear the CMOS then load and save Optimal Values in the BIOS.

Question: **After flashing the BIOS my system does not have video. How can I correct this?**
Answer: Normally, if you do not have video after flashing your BIOS this indicates the flashing procedure failed. To remedy this, first clear the CMOS per instructions in this manual and retry. If you still do not have video, please use the following BIOS recovery procedure. Turn your system off and place the floppy disk with the saved BIOS image file (see above FAQ) in drive A. On your keyboard press and hold "CTRL" and "Home." Turn on power with the hot keys depressed until your floppy drive is accessed. Your screen will remain blank until the BIOS program block is flashed. If your system either rebooted or displays a message to reboot the system then the procedure was successful.

Question: **I have memory problems. What is the correct memory to use and is there any BIOS setting that may help me?**
Answer: The correct memory to use on the P6SLA/P6SLE is 168-pin DIMM non-buffered SPD (Serial Present Detection) SDRAM, SDRAM and EDO memory. SPD SDRAM is preferred but is not necessary. IMPORTANT: Please do not mix memory types; the results are unpredictable. If your memory count is exactly half of the correct value, please go to the BIOS in Chipset Setup and select "SDRAM AUTOSIZING SUPPORT." Change between available options until one setting correctly displays your memory.

Question: **Which Operating System (OS) supports AGP?**
Answer: At present Windows 98 and Windows NT 5.0 are the only OS that will have built-in support for AGP. Some AGP video adapters can run Windows 95 OSR2.1 with special drivers. Please contact your graphics adapter vendor for more details.

Question: **Do I need the compact disk that came with your motherboard?**
Answer: The supplied compact disc has quite a few drivers and programs that greatly enhance your system. We recommend that you review the compact disc and use what you desire. Some of the items packaged on the compact disc are PCI IDE Bus Master drivers for Windows 95 and Windows NT, 440LX chipset drivers for Windows 95, and Super Doctor Monitoring software.

Question: **Why can't I turn off the power using the momentary power on/off switch?**
Answer: The instant power off function is controlled by the BIOS. When this feature is enabled in the BIOS, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When this feature is disabled or when the BIOS is not in control, such as during memory count, the momentary on/off switch must be held for five seconds before the system will shut down. These changes were necessary to implement ACPI features on the motherboard.

Question: **I see a few of my PCI devices sharing IRQs. The system seems to be fine, but is this acceptable?**
Answer: Some PCI Bus Mastering devices can share IRQs without performance penalties. These devices are designed to work correctly sharing IRQs.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alteration, misuse, abuse, or improper maintenance of products.

Chapter 4
AMI BIOS

4-1 Introduction

This chapter describes the AMIBIOS for the Intel 440LX Pentium II 233/266/300/333 MHz processors. The AMI ROM BIOS is stored in the Flash EEPROM and is easily upgraded using a floppy disk-based program.

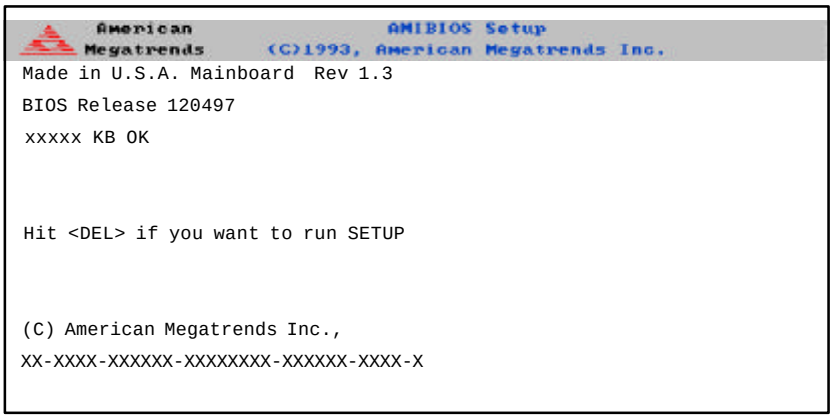
System BIOS
The BIOS is the basic input output system used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. The WinBIOS is a high-quality example of a system BIOS.

Configuration Data
AT-compatible systems, also called ISA (Industry Standard Architecture) must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

How Data Is Configured
AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM.

POST Memory Test
Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown on the next page.

An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message.



4-2 BIOS Features

- supports Plug and Play V1.0A and DMI 2.0
- supports Intel PCI 2.1 (Peripheral Component Interconnect) local bus specification
- supports EDO (Extended Data Out), ECC and FPM DRAM
- supports ECC (Error Checking and Correction)
- supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- can be used as a boot device
- is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- CPU temperature
- additional temperature sensors

- chassis intrusion detector
- five positive voltage inputs
- two negative voltage inputs
- three fan speed monitoring inputs

BIOS Configuration Summary Screen
AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

AMIBIOS System Configuration (C) 1985-1994 American Megatrends Inc.,			
Main Processor	: Pentium(tm) II	Base Memory Size	: 640 KB
Math Processor	: Built-In	Ext. Memory Size	: 31744 KB
Floppy Drive A:	: 1.2 MB, 5¼	Display Type	: VGA/EGA
Floppy Drive B:	: 1.44 MB, 3½	Serial Port(s)	: 3F8, 2F8
AMI-BIOS Date	: 7/15/95	Parallel Port(s)	: 378
Processor Clock	: 300MHz	Power Management	: APM, SMI

AMIBIOS Setup
See the following page for examples of the AMIBIOS Setup screen, featuring options and settings. Figure 4-1 shows the ***Standard*** option highlighted. To highlight other options, use the arrow keys, or use the tab key to move to other option boxes. Figure 4-2 shows the settings for the Standard setup. Settings can be viewed by highlighting a desired option and pressing <Enter>. Use the arrow keys to choose a setting. Note: Optimal settings for all options can be set automatically. Go to the ***Optimal*** icon in the default box and press <Enter>. Use the arrow keys to highlight *yes,* then press <Enter>.

Upgrading the BIOS
Flash BIOS update information: ***Please note that you cannot use Super P6SLA rev. 1 and 2 board BIOS upgrades on a rev. 3 motherboard.*** Using the inappropriate BIOS upgrade will make your system inoperative and the BIOS chip will need to be replaced. Please ensure you have the correct BIOS code before updating your system. Visit our web site at www.supermicro.com and go to the BIOS download area for upgrades and for further information.

Figure 4-1. Standard Option Highlighted

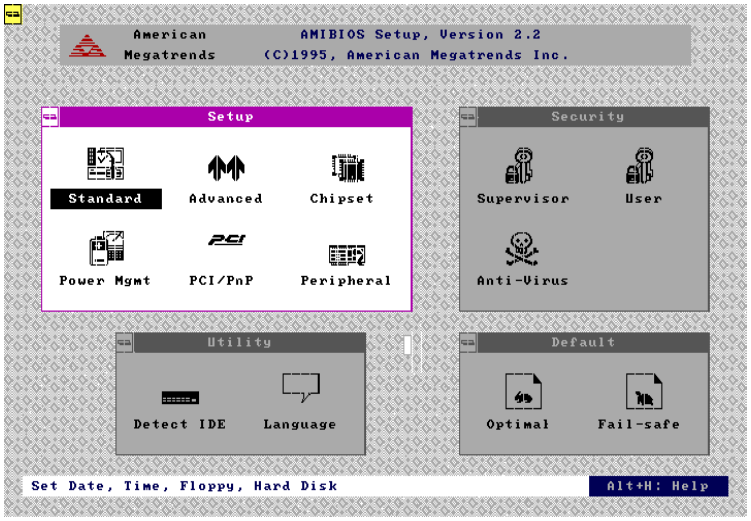
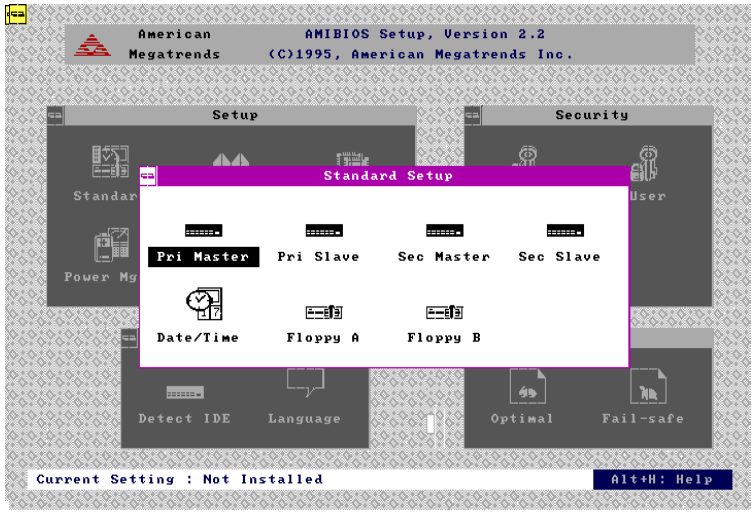


Figure 4-2. Settings for Standard Option



Chapter 5
Running Setup*

Optimal and Fail-Safe default settings are bolded in text unless otherwise noted.

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the option.

5-1 Setup

5-1-1 Standard Setup

Pri Master
Pri Slave
Sec Master
Sec Slave

Choose these icons to configure the hard disk drive. When you click on an icon, the following parameters are listed: *Type, LBA/ Large Mode, Block Mode, 32Bit Mode, and PIO Mode*. All parameters relate to IDE drives except *Type*.

If the hard disk drive to be configured is an IDE drive, select the appropriate drive icon, choose the *Type* parameter and select ***Auto***. The BIOS will automatically detect the IDE drive parameters and display them. Click on the OK button to accept these parameters.

Click on *LBA/Large Mode* and choose *On* to enable support for IDE drives with capacities greater than 528MB. Click on *Block Mode* and choose *On* to support IDE drives that use Block Mode. Click on *32Bit Mode* and click on *On* to support IDE drives that permit 32-bit accesses.

To configure an old MFM hard disk drive, you must know the drive parameters (number of heads, number of cylinders, number of sectors, the starting write precompensation cylinder, and drive capacity). Select the hard disk drive type (1-46). Refer to table below.

AMI BIOS Hard Disk Drive Types

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Size
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	831	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB
47	ENTER PARAMETERS PROVIDED WITH HARD DRIVE					

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads will normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drive may have even more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Date and Time Configuration

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values through the keyboard.

Floppy A
Floppy B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are ***Not Installed***, *360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch* or *2.88 MB 3½ inch*.

5-1-2 Advanced Setup

Quick Boot
Set this option to Enabled to permit AMIBIOS to boot within 5 seconds. The Settings are ***Disabled*** or *Enabled*.

Pri Master ARMD Emulated as
Pri Slave ARMD Emulated as
Sec Master ARMD Emulated as
Sec Slave ARMD Emulated as
Options for Pri Master ARMD Emulated as, Pri Slave ARMD Emulated as, Sec Master ARMD Emulated as and Sec Slave ARMD Emulated as are ***Auto****, Floppy and Hard disk*.

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device
The options for 1st Boot Device are *Disabled, 1st IDE-HDD, 2 IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD,* ***Floppy****, ARMD-FDD, ARMD-HDD, ATAPI CD ROM, SCSI, Network* or *I_2O*. The options for 2nd Boot Device are *Disabled,* ***1st IDE-HDD****, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or ATAPI*. The options for 3rd Boot Device are *Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or* ***ATAPI CD ROM***. The options for the 4th Boot Device are ***Disabled****, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD*. The *Disabled* option in the 4th boot device means that setup will not be considered during the boot process.

1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD and 4th IDE-HDD are the four hard disks than can be installed by the BIOS. 1st IDE-HDD is the first hard disk installed by the BIOS, 2nd IDE-HDD is the second hard disk, and so on. For example, if the system has a hard disk connected to Primary Slave and another hard disk to Secondary Master, then 1st IDE-HDD will be referred to as the hard disk connected to Primary Slave and 2nd IDE-HDD will be referred to as the hard disk connected to the Secondary Master. 3rd IDE-HDD and 4th IDE-HDD are not present. Note that the order of the initialization of the devices connected to the primary and secondary channels are Primary Master first, Primary Slave second, Secondary Master third, and Secondary Slave fourth.

The BIOS will attempt to read the boot record from 1st, 2nd, 3rd and 4th boot device in the selected order until it is successful in reading the booting record. The BIOS will not attempt to boot from any device which is not selected as the boot device.

Try Other Boot Device
This option controls the action of the BIOS if all the selected boot devices failed to boot. The settings for this option are ***Yes*** or *No*. If *Yes* is selected and all the selected boot devices failed to boot, the BIOS will try to boot from the other boot devices (in a pre-defined sequence) which are present but not selected as boot devices in the setup (and hence not yet been tried for booting). If selected as *No* and all selected boot devices failed to boot, the BIOS will try not to boot from the other boot devices which may be present but not selected as boot devices in setup.

Initial Display Mode
This option determines the display screen with which the POST is going to start the display. The settings for this option are ***BIOS*** or *Silent*. If selected as *BIOS,* the POST will start with the normal sign-on message screen. If *Silent* is selected, the POST will start with the silent screen.

Display Mode at Add-on ROM Init
This option determines the display mode during add-on ROM (except Video add-on ROM) initialization. The settings for this option are ***Force BIOS*** or *Keep Current*. If selected as *Force BIOS,* the POST will force the display to be changed to BIOS mode before giving control to any add-on ROM. If no add-on ROM is found, then the current display mode will remain unchanged even if this setup question is selected as *Force BIOS.* If selected as *Keep Current,* then the current display mode will remain unchanged.

Floppy Access Control
The settings for this option are ***Read-Write*** or *Read-Only*.

Hard Disk Access Control
The settings for this option are ***Read-Write*** or *Read-Only*.

S.M.A.R.T. for Hard Disks
S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a technology developed to manage the reliability of the hard disk

by predicting future device failures. The hard disk needs to be S.M.A.R.T. capable. The settings for this option are ***Disabled*** or *Enabled*. ***Note: SMART cannot predict all future device failures. SMART should be used as a warning tool, not as a tool to predict the device reliability.***

Boot Up Num-Lock
Settings for this option are ***On*** or *Off*. When this option is set to *On*, the BIOS turns off the Num Lock key when the system is powered on. This will enable the end user to use the arrow keys on both the numeric keypad and the keyboard.

PS/2 Mouse Support
Settings for this option are ***Enabled*** or *Disabled*. When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse.

Primary Display
This option specifies the type of display adapter card installed in the system. The settings are *Absent,* ***VGA/EGA***, *CGA40x25*, *CGA80x25* or *Mono*.

Password Check
This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if WinBIOS Setup is executed.

Boot to OS/2
If DRAM size is over 64 MB, set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are ***No*** or *Yes*.

CPU MicroCode Updation
The settings for this option are *Disabled* or ***Enabled***. Set this option to *Enabled* to allow the CPU microcode to be updated online at any time.

Internal Cache
This option is for enabling or disabling the internal cache memory. The settings for this option are *Disabled, WriteThru* or ***WriteBack***.

System Bios Cacheable
AMIBIOS always copies the system BIOS from ROM to RAM for faster execution. The settings are *Disabled* or ***Enabled***. *Note: the Fail-Safe default setting is* ***Disabled****.* Set this option to *Enabled* to permit the contents of F0000h RAM memory segment to be written to and read from cache memory.

C000, 16K Shadow
C400, 16K Shadow
These options specify how the contents of the video ROM are handled. The settings are: *Disabled*, *Enabled or* ***Cached***. When set to *Cached*, the contents of the video ROM area from C0000h-C7FFFh are not only copied from ROM to RAM, the contents of the C0000h-C7FFFh RAM can be written to or read from cache memory.

C800, 16K Shadow
CC00, 16K Shadow
D000, 16K Shadow
D400, 16K Shadow
D800, 16K Shadow
DC00, 16K Shadow
These options specify how the contents of the adaptor ROM named in the option title are handled. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards. The settings are: ***Disabled****, Enabled or Cached*.

5-1-3 Chipset Setup

USB Function
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the USB (Universal Serial Bus) functions.

USB KB/Mouse Legacy Support
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the USB keyboard and mouse.

SDRAM Autosizing Support
If the Serial Presence Detect (SPD) is not available, then the BIOS will try to detect the memory and do the autosizing. The settings for this option are ***Auto****, Enabled* or *Disabled*.

EDO DRAM Speed (ns)
This option should be set according to the speed of the EDO DRAM in the system. The value of this option determines how the EDO DRAM timings should be programmed in the chipset. The settings for this option are ***Auto****, Manual*, *50, 60* or *70*.

EDO Read Burst Timing
Burst mode EDO have internal column counters. Because of this, they do not need to accept row addresses and starting column addresses from the EDO memory controller. This eliminates the setup and hold time for the second and subsequent column addresses. It also improves the EDO Read access time. The settings for this option are ***x333*** or *x222*.

EDO Write Burst Timing
Burst mode EDO have internal column counters. Because of this, they do not need to accept row addresses and starting column addresses from the EDO memory controller. This eliminates the setup and hold time for the second and subsequent column addresses. It also improves the EDO Write access time. The settings for this option are ***x333*** or *x222*.

EDO RAS Precharge
Memory needs to be recharged to ensure the information stored is not lost. This feature eliminates the RAS (Row Address Strobe) recharge time since memory must always be addressed in the order of Row first, then Column. The settings for this option are ***4 Clks*** or *3 Clks*.

EDO RAS to CAS
As previously described, memory must always be addressed in the order of Row, then Column. The EDO RAS to CAS feature sets the timing delay between Row addressing and Column addressing. The settings for this option are ***3 Clks*** or *2 Clks*.

MA Waitstate
Use this feature to configure the memory address wait state. The settings for this option are ***Slow*** or *Fast*.

SDRAM Timing Latency
Use this feature to select the SDRAM timing delay. The settings for this option are *Manual* or ***Auto***.

SDRAM RAS to CAS
The settings for this option are ***3 Clks*** or *2 Clks*.

SDRAM CAS Lat
This feature is for the Column Address Strobe latency. The settings for this option are ***3 Clks*** or *2 Clks*.

SDRAM RAS Precharge
This feature is for the SDRAM Row Address Strobe delay. The settings for this option are ***3 Clks*** or *2 Clks*.

VGA Frame Buffer USWC
USWC is a memory cycle type that stands for Uncacheable Speculative Write Combining. The settings are: ***Disabled*** or *Enabled*.

PCI Frame Buffer USWC
The settings for this option are: ***Disabled*** or *Enabled*. When *Enabled,* the PCI frame buffer address and length are divided into 2. The value is then programmed into the processor Variable MTRR (3) with the value for USWC (01h).

DRAM Integrity Mode (ECC)
The settings for this option are: ***Non ECC***, *EC only* or *ECC*. Set this option to *Enabled* to enable ECC DRAM integrity mode. ECC allows critical system to detect and correct memory errors, while normal parity generator/checker can only detect such memory errors.

Fixed Memory Hole
This option allows a memory hole to be specified for either the 512-640K region or the 15-16M region. The settings for this option are ***Disabled***, *512-640KB* or *15-16MB*.

Type F DMA Buffer Control 1
Type F DMA Buffer Control 2
Instead of 8 sysclock, Type F DMA only requires 3 sysclock to finish the data transfer. These two options are device dependent. The settings are *Channel 0*, *Channel 1, Channel 2,* ***Disabled****, Channel 3, Channel 5, Channel 6 or Channel 7.*

DMA-0 Type
DMA-1 Type
DMA-2 Type
DMA-3 Type
DMA-5 Type
DMA-6 Type
DMA-7 Type
The settings for these Direct Memory Access channels are ***Normal ISA***, *PC/PCI* or *Distributed*.

AGP Aperture Size
This register determines the effective size of the Graphics Aperture used in the particular PAC configuration. This register can be updated by the PAC-specific BIOS configuration sequence before PCI standard bus enumeration sequence takes place. If the register is not updated, a default value selects aperture of maximum size (i.e., 256 MB). The settings are: *4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB* or ***256 MB***.

System Type
The settings are: ***Auto****, DP* or *UP*.

USWC Write I/O Post
Use this feature for the WC Write Post During I/O Bridge Access Enable (WPIO). When set to *Enabled,* posting of WC transactions to PCI occur, even if the I/O bridge has been granted access to the PCI bus via corresponding arbitration and buffer management protocol. USWC Write posting should only be enabled if a USWC region is located on the PCI bus. The settings are: ***Auto****, Disabled* or *Enabled*.

MAA 1:0 Buf. Strength
MECC Buf. Strength
MD Buf. Strength
RCSA0/RCSB0 Buf. Strength
MAB 1:0 Buf. Strength

MAA 13.2 Bufl Strength
RCSA1/RCSB1 Buf. Strength
RCSA2/RCSB2 Buf. Strength
RCSA3/RCSB3 Buf. Strength
RCSA4/RCSB4 Buf. Strength
CDQB 5,1 Buf. Strength
CDQA 5,1 Buf. Strength
CDQA 0, 2:4, 6:7 Buf. Strength
RCSA5/RCSB5 Buf. Strength
RCSA6/RCSB6 Buf. Strength
RCSA7/RCSB7 Buf. Strength

The above features control the memory buffer strength. They are used to program the various DRAM interface signal buffer strengths, based on memory configuration, DRAM type (EDO or SDRAM), DRAM density (x4, x8, x16, or x32), DRAM technology (16 Mb or 64 Mb), and rows populated. *Note the Optimal and Fail-Safe default settings are* ***Auto.***

PAC Bus SERR#

The settings for this option are: *Disabled* or ***Enabled***. When set to *Enabled*, the PAC's SERR# signal driver is enabled and SERR# is asserted for all relevant bits set in the ERRSTS and PCISTS as controlled by the corresponding bits of the ERRCMD register. When *Disabled*, SERR# is never driven by the PAC.

AGP Common SERR#

The settings are: *Disabled* or ***Enabled***. Set to *Enabled* to permit a common SERR# signal for AGP and the standard PCI bus.

AGP System Error Forwarding

The settings are: *Disabled* or ***Enabled***. Set this option to *Enabled* to enable AGP systems errors to be forwarded.

AGP Parity Error Response

The settings are: *Disabled* or ***Enabled***. Set this option to *Enabled* to enable AGP parity error response.

IRQ12

The settings are: ***Auto****, Standard* or *Mouse*. When this option is set to *Auto* the AMIBIOS automatically determines how IRQ12 should be allocated. In the *Standard* setting IRQ12 is made available for use on the ISA bus. IRQ12 is used by the PS/2 Mouse, when in *Mouse* setting.

PIIX4 SERR#
Use this feature for the SERR# generation due to delayed transaction time-out enable. The settings are: ***Disabled*** or *Enabled*.

USB Passive Release Enable
The settings for this option are: *Disabled* or ***Enabled***. When set to *Enabled,* it allows the PIIX4 to use Passive Release while transferring control information or data for USB transactions. When *Disabled,* PIIX4 will perform PCI accesses for USB without using Passive Release.

PIIX4 Passive
Use the PIIX4 Passive feature to enable the Passive Release mechanism encoded on the PHOLD# signal when PIIX4 is a PCI master. The settings are: *Disabled* or ***Enabled***.

PIIX4 Delayed Transaction
Use this feature to enable the Delayed Transaction mechanism when the PIIX4 is the target of a PCI transaction. The settings are: *Disabled* or ***Enabled***.

Master Lat. Timer
Master Latency Timer is an 8-bit register that controls the amount of time the PAC, as a PCI bus master, can burst data on the PCI bus. The count value is an 8 bit quantity. However, MLT[2:0] are 0 when determining the count value. The PAC's MLT is used to guarantee to the PCI agents (other than PAC) a minimum amount of the system resources. *Note: Settings are in increments with an Optimal and Fail-Safe default setting of* ***40H****.*

MTT
Multi-Transaction Timer is an 8-bit register that controls the amount of time that the PAC's arbiter allows a PCI initiator to perform multiple back-to-back transactions on the PCI bus. The PAC's MTT mechanism is used to guarantee the fair share of the PCI bandwidth to an initiator that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it cannot use long burst transfers). *Note: Settings are in increments with an Optimal and Fail-Safe default setting of* ***20H***.

5-1-4 Power Management

ACPI Aware OS
Use this feature if your operating system supports Microsoft's Advanced Configuration and Power Interface (ACPI) standard. The settings are: *Yes* or ***No***.

Power Management/APM
This power conservation feature is specified by Intel and Microsoft

settings are: ***Disabled*** *Enabled*. When this feature is set to the system power conservation features are controlled by the system BIOS, not by the operating system.

Power Button Function
This feature is used to select the functionality of the power supply's power button. The settings are: or ***On/Off***

The settings for power supply type are ***AT*** *or ATX.*

Instant on Support

back on instantly from ACPI's SoftOff state. The settings are: ***Disabled*** or *Enabled*.

Green PC Monitor Power State
This option specifies the power state that the green PC-compliant

The settings are ***Standby***, *Suspend* or *Off*.

Video Power Down Mode
This option specifies the power conserving state that the VGA video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or ***Suspend***.

Hard Disk Power Down Mode
This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are *Disabled*, *Standby*, or ***Suspend***.

Hard Disk Timeout (Minutes)
This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters power-conserving state specified in the Hard Disk Power Down Mode option. The settings are ***Disabled*** and *1 Min through 15 Min in 1 minute intervals*.

Standby/Suspend Timer Unit
This allows you to set the standby time out and suspend time out timer unit. The settings are *32 secs*, *4 msecs*, ***4 min*** or *4 secs.*

Standby Time Out
This option specifies the length of a period of system inactivity while in full power on state. When this length of time expires, the computer enters standby power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Suspend Timeout (Minutes)
This option specifies the length of a period of system inactivity while in standby state. When this length of time expires, the computer enters suspend power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Slow Clock Ratio
The value of the slow clock ratio indicates the percentage of time the STPCLK# signal is asserted while in the thermal throttle mode. The settings are ***Disabled****, 12.5%*, *25%*, *37.5%*, *50%*, *62.5%*, *75%*, and *87.5%*.

Display Activity
This option specifies if AMIBIOS is to monitor display activity for power conservation purposes. When this option is set to *Monitor* and there is no display activity for the length of time specified in the Standby Timeout (Minute) option, the computer enters a power savings state. The settings are *Monitor* or ***Ignore***.

Device 6 (Serial port 1)
Device 7 (Serial port 2)
Device 8 (Parallel port)
Device 5 (Floppy disk)
Device 0 (Primary Master IDE)
Device 1 (Primary Slave IDE)
Device 2 (Secondary Master IDE)

Device 3 (Secondary Slave IDE)

These options are for event monitoring. The settings for each of these options are Monitor or ***Ignore***.

LAN Wake-Up
RTC Wake-UP
Hour
Minute

Options for LAN Wake-Up and RTC Wake-Up are ***Disabled*** and *Enabled*. *Note: The optimal setting for Hour and Minute is* ***N/A***. There is no fail-safe setting for *Hour* and *Minute.*

5-1-5 PCI/PnP Setup

Plug and Play-Aware OS

The settings for this option are *Yes* or ***No***. Set this option to *Yes* if the operating system in the computer is aware of and follows the Plug and Play specification. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. Currently, only Windows 95 is PnP-Aware. Set this option to *No* if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly. Otherwise, PnP-aware adapter cards installed in the computer will not be configured properly.

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings in PCI clocks for all PCI devices. The settings are *32*, ***64***, *96*, *128*, *160*, *192*, *224*, or *248*.

PCI VGA Palette Snoop

The settings for this option are ***Disabled*** or *Enabled.* When set to *Enabled,* multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example: if there are two VGA devices in the computer (one PCI and one ISA) and this option is disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers. If enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA palette registers. This will permit the palette regis-

ters of both devices to be identical. This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping.

PCI IDE Busmaster
The settings are: ***Disabled*** or *Enabled*.

Offboard PCI IDE Card
This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. The PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed must be specified. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are ***Auto*** (AMIBIOS automatically determines where the offboard PCI IDE controller adapter card is installed), *Slot 1*, *Slot 2*, *Slot 3*, *Slot 4, Slot 5* or *Slot 6*.

This option forces IRQ14 and IRQ15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant ISA IDE controller adapter cards. If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

Offboard PCI IDE Primary IRQ
Offboard PCI IDE Secondary IRQ
These options specify the PCI interrupt used by the primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are ***Disabled***, *Hardwired*, *INTA*, *INTB*, *INTC*, or *INTD*.

PCI Slot1 IRQ Priority
PCI Slot2 IRQ Priority
PCI Slot3 IRQ Priority
PCI Slot4 IRQ Priority
These options specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are ***Auto****, (IRQ) 3, 4, 5, 7, 8, 10, and 11, in priority order****.***

DMA Channel 0
DMA Channel 1
DMA Channel 3
DMA Channel 5
DMA Channel 6
DMA Channel 7

These DMA channels control the data transfers between the I/O devices and the system memory. The chipset allows the BIOS to choose which channels to do the job. The settings are ***PnP*** or *ISA/EISA.*

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15

These options specify which bus the specified IRQ line is used on and allow you to reserve IRQs for legacy ISA adapter cards. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an ISA/EISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP.

IRQ14 and 15 will not be available if the onboard PCI IDE is enabled. If all IRQs are set to ISA/EISA and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ 9 will still be available for PCI and PnP devices. This is because at least one IRQ must be available for PCI and PnP devices. The settings are ***PCI/PnP*** or *ISA/EISA.*

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are ***Disabled***, *16K*, *32K,* or *64K*.

Reserved Memory Address
This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are *C0000*, *C4000*, *C8000*, *CC000*, *D0000*, *D4000*, ***D8000***, or *DC000*.

5-1-6 Peripheral Setup

OnBoard FDC
This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are ***Auto*** (AMIBIOS automatically determines if the floppy controller should be enabled), *Disabled*, or *Enabled*.

OnBoard Serial Port 1
This option specifies the base I/O port address of serial port 1. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h*, *2F8h*, *3E8h*, or *2E8h*.

OnBoard Serial Port 2
This option specifies the base I/O port address of serial port 2. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h*, *2F8h*, *3E8h*, or *2E8h*.

Serial Port 2 Mode
The settings are ***Normal****, Sharp-IR, IrDA,* or *TV Remote.*

IR Duplex Mode
The settings are *Half* or *Full. Note: The Optimal and Fail-Safe default settings are* ***N/A***.

IR Receiver Pin
The settings are *IRRX1* or *IRRX2. Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

OnBoard Parallel Port
This option specifies the base I/O port address of the parallel port on the motherboard. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *378*, *278*, or *3BC*.

Parallel Port Mode
This option specifies the parallel port mode. The settings are *Normal*, ***Bi-Dir***, *EPP* or *ECP*. When set to *Normal,* the normal parallel port mode is used. Use *Bi-Dir* to support bidirectional transfers. Use *EPP* (Enhanced Parallel Port) to provide asymmetric bidirectional data transfer driven by the host device. Use *ECP* (Extended Capabilities Port) to achieve data transfer rates of up to 2.5 Mbps. ECP uses the DMA protocol and provides symmetric bidirectional communication.

EPP Version
The settings are *1.7* or *1.9. Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

Parallel Port IRQ
This option specifies the IRQ to be used by the parallel port. The settings are ***Auto***, *5* or *7*.

Parallel Port DMA Channel
This option is only available if the setting of the parallel port mode option is ECP. The settings are *0*, *1*, *2*, *3*, *5*, *6* or *7*. *Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

OnBoard IDE
This option specifies the onboard IDE controller channels to be used. The settings are *Disabled, Primary*, *Secondary*, or ***Both***.

OnBoard NAT307 Mode Set
The settings for this option are ***Non-PnP*** and *PnP*.

OnBoard SCSI
Enable the OnBoard SCSI feature to use the onboard SCSI on the motherboard. The settings are *Disabled* or *Enabled*. *Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

Remote Power On
Microsoft's Memphis OS supports this feature which can wake-up the system from SoftOff state through devices (such as an external modem) that are connected to COM1 or COM2. The settings are ***Disabled*** or *Enabled*.

AC Power Lost Restart: Disabled
The settings for this option are ***Disabled***.

CPU Current Temperature
The current CPU temperature is displayed in this option.

CPU Overheat Warning Temperature
Use this option to set the CPU overheat warning temperature. The settings are *25 ◦C through 75 ◦C in 1 ◦C intervals*. *Note: The Optimal and Fail-Safe default settings are* ***55 ◦C***.

CPU Overheat Clock Down
The CPU internal clock will slow down to the specified frequency percentage when it is overheated. The settings are ***Disabled***, *12.5%, 25%, 37.5%, 50%, 62.5%, 75%* or *87.5%*.

LM78 In0 (CPU 1)
LM78 In1 (CPU 2)
LM78 In2 (+3.3V)
LM78 In3 (+5V)
LM78 In4 (+12V)
LM78 In5 (-12V)
LM78 In6 (-5V)
CPU1 Fan
CPU2 Fan
Chassis Fan
The above features are for PC Health Monitor W83781D. The motherboards with W83781D have seven onboard voltage monitors for the CPU core, CPU I/O, +3.3V, +5V, -5V, +12V, and -12V, and three fan status monitors.

5-2 Security Setup

5-2-1 Supervisor User

The system can be configured so that all users must enter a password every time the system boots or when the WINBIOS setup is executed. You can set either a Supervisor password or a User password. If you do not want to use a password, just press <Enter> when the password prompt appears.

The password check option is enabled in the Advanced Setup by choosing either *Always* or *Setup*. The password is stored in CMOS RAM. You can enter a password by typing the password on the keyboard, selecting each letter via the mouse, or selecting each letter via the pen stylus. Pen access must be customized for each specific hardware platform.

When you select Supervisor or User, AMIBIOS prompts for a password. You must set the Supervisor password before you can set the User password. Enter a 1-6 character password. The password does not appear on the screen when typed. Retype the new password as prompted and press <Enter>. Make sure you write it down. If you forget it, you must drain CMOS RAM and reconfigure.

5-2-2 Anti-Virus

When this icon is selected, AMIBIOS issues a warning when any program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive. The settings are *Enabled* or ***Disabled***.

5-3 Utility Setup

5-3-1 Language

Note: The Optimal and Fail-Safe default settings for this option are ***English****.*

5-3-2 Detect IDE

Use this icon to let the BIOS autodetect the IDE hard drive.

5-4 Default Setting

Every option in WinBIOS Setup contains two default settings: a Fail-Safe default, and an Optimal default.

5-4-1 Optimal Default

The Optimal default settings provide optimum performance settings for all devices and system features.

5-4-2 Fail-Safe Default

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Appendix A
BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error was detected in the base memory (the first 64 KB block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64 KB of memory.
4	Timer Not Operational	A memory failure was detected in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU on the system board generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error means that the BIOS cannot switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the motherboard generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. ***Please Note:*** This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS memory has failed.
11	Cache memory bad - do not enable cache	The cache memory test failed. Cache memory is disabled. ***Do not press <Ctrl>+<Alt>+<Shift> and <+> to enable cache memory.***

Refer to the table on page A-3 for solutions to the error beep codes.

If it beeps...	**then ...**
1, 2, 3 times	reseat the memory SIMMs or DIPs. If the system still beeps, replace the memory.
6 times	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
11 times	reseat the cache memory on the motherboard. If it still beeps, replace the cache memory.
4, 5, 7, or 10 times	the motherboard must be replaced.

Appendix B

AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMI BIOS.

Check Point	Description
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next.
03	NMI is Disabled. Next, checking for a soft reset or a power-on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the post code unit next.
07	Next, initializing the CPU init and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before keyboard BAT command is issued.
0C	The keyboard controller I/B is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0F	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.

Check Point	Description
10	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh test line is toggling. Checking the 15 second on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG Switch is on.
27	Any initialization before setting video mode will be done next.

Check Point	Description
28	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30	The display memory read/write test passed. Look for retrace checking next.
31	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.

Check Point	Description
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error messages.
3A	The new cursor position has been read and saved. Displaying the Hit <DEL> message next.
40	Preparing the descriptor tables next.
42	The descriptor tables are prepared. Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been completed. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4B	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.

Check Point	Description
4C	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4D	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4F	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next.
59	The Hit <DEL> message is cleared. The <WAIT> message is displayed. Starting the DMA and interrupt controller test next.

Check Point	Description
60	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
7F	Extended NMI source enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	The command byte was written and global data initialization has been completed. Checking for a locked key next.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86	The password was checked. Performing any required programming before WINBIOS Setup next.

Check Point	Description
87	The programming before WINBIOS Setup has been completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89	The programming after WINBIOS Setup has been completed. Displaying the power-on screen message next.
8B	The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the WINBIOS Setup options next.
8D	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8F	The hard disk controller has been reset. Configuring the floppy drive controller next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has been completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.

Check Point	Description
99	Any initialization required after the option ROM test has been completed. Configuring the timer data area and printer base address next.
9A	Set the timer and printer base addresses. Setting the RS-232 base address next.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	The soft error display has completed. Setting the keyboard typematic rate next.
A4	The keyboard typematic rate is set. Programming the memory wait states next.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.

Check Point	Description
A9	Returned from adaptor ROM at E000h control. Next, performing any initialization required after the E000 option ROM had control.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary. POST next.
B0	The system configuration is displayed.
AC	Uncompressing the DMI data and initializing DMI.
B1	Copying any code to specific areas.