PEM-3301

Cache-386 33MHz Mainboard User's Manual

Edition 1 .01

Warning

Reconfiguring

NEVER reconfigure the board while the power is ON.

If you wish to reconfigure the board at any time, make sure that the power is turned OFF before changing any hardware settings, such as DIP switches or jumpers.

Checklist

Your PEM-3301 mainboard package contains the following:

- One PEM-3301 Mainboard
- One User's Manual
- One System Setup Program Manual (optional for DTK BIOS user)
- One utility diskette

Contents

The 80386-based PEM-3301 mainboard ensures superlative performance and complete compatibility with software written for IBM PC/AT 80286-type and 80386-type processors.

The PEM-3301 uses a cache memory subsystem providing a small amount of fast memory (SRAM) and a large amount of slow memory (DRAM). This system is configured to so that all system memory is fast memory and is fast enough to complete bus cycles with no wait states. The cache memory provides high performance with a cost approaching that of DRAM.

The clear, well-illustrated instructions in this manual ensure that even if you are a newcomer to the computer world, you will have your system installed and running with a minimum of effort.

A brief description of the PEM-3301 is given below:

- Intel 80386-33 microprocessor with Intel 80387-33 or Weitek 3167 numeric coprocessor optional
- Dual speed, 33MHz cache support in ultra-high speed and emulatiion without cache in low speed, both switchable by either software or hardware switches
- Discrete components to complete cache functions
- 1/2/4/5/8 MB 32-Bit DRAM onboard
- 64/256 KB direct-mapped high-speed SRAM cache memory
- Write-Back cache update for O-wait state memory-write operations
- DTK, Phoenix, Award, or AMI BIOS support
- Shadow RAM function for BIOS and video
- One 32-bit memory expansion slot for PEI-306 32-bit memory expansion card to expand 32-bit memory up to 16MB
- Six 16-bit AT compatible I/O slots
- Two 8-bit AT compatible I/O slots
- Standard 8MHz AT bus speed
- DALLAS DS1 287 chip to maintain system configuration and real time clock setting
- Keyboard and speaker attachments
- Seven DMA channels
- 16 level interrupt
- Three programmable timers
- System performance rated by:
  Landmark (V. 0.99): 55.9 — 58.7 and
  Power Meter MIPS (V. 1.5): 8.171 MIPS

The PEM-3301 uses an Intel 80386-33 microprocessor running at 33MHz.

The Intel 80386 is a high-performance 32-bit microprocessor designed for multitasking operating systems. The processor can address up to 4 gigabytes of physical memory and 64 terabytes of virtual memory.

It incorporates integrated memory management and protection in its architecture in the form of address-translation registers, advanced multitasking hardware, and a protect mechanism to support operating systems. In addition, its object code is compatible with the 8086 family of microprocessors.

The 80386 has built-in features to support coprocessors, DMA and interrupts (both maskable and non-maskable). It has two modes of operation: Real Address mode and the Protected Virtual Address mode.

In Real Address mode, the 80386 operates as a fast 8086 with a 32-bit extension if necessary. The Protected Virtual Address mode is the natural environment of the 80386. Software can perform a task switch into tasks designated as virtual 8086 mode tasks. Virtual 8086 tasks can be isolated and protected from one another by use of paging and I/O-permission bit mapping.

Math Coprocessor

The PEM-3301 mainboard supports the Intel 80387 and the Weitek 3167 numeric coprocessors to accelerate processing of calculation-intensive tasks.

Cache Algorithm

In a cache memory system, all data are stored in main memory and some data are duplicated in the cache. When the processor accesses memory, it checks the cache first. If the desired data are in the fast-memory cache, the processor can access the data quickly. If the desired data are not in the cache, the data must be fetched from main memory. If the requested data are found in the cache, the memory access is called a cache hit; if not, it is called a cache miss. The hit rate is the percentage of accesses that are hits; it is affected by the size and physical organization of the cache, the cache algorithm, and the program being run.

The following section describes the cache algorithm of the PEM-3301.

Cache Organization — Direct-Mapped Cache

The direct-mapped cache memory is an alternative to associative-cache memory, which uses a single address comparator for the memory system and standard RAM cells for the address and data cells. The direct-mapped cache is based on an idea borrowed from software called hash coding.

This is a method for simulating an associative memory. In the hash coding approach, the memory address space is divided into a number of sets of words with the goal of each set having no more than one word of most-frequently-used data.

Each direct-mapped cache address has two parts. The first part, called the cache index field, contains enough bits to specify a block location within the cache. The second field, called the tag field, contains enough bits to distinguish one block from other blocks that may be stored at a particular location.

For example, consider a 64KB direct-mapped cache that contains 16K 32-bit locations and caches 16MB of main memory. The cache index field must include 14 bits to select one 16K block in the cache, plus 2 bits to select a byte from the 4-byte sub-block. The tag field must be 8 bits wide to identify one of the 256 blocks that can occupy the selected cache location. Therefore, the system requires 64KB of cache RAM (16K 4-byte sub-blocks) to hold the data and code and 16K of 8 bit RAM to hold the tag. The direct-mapped cache organization is shown as follows.

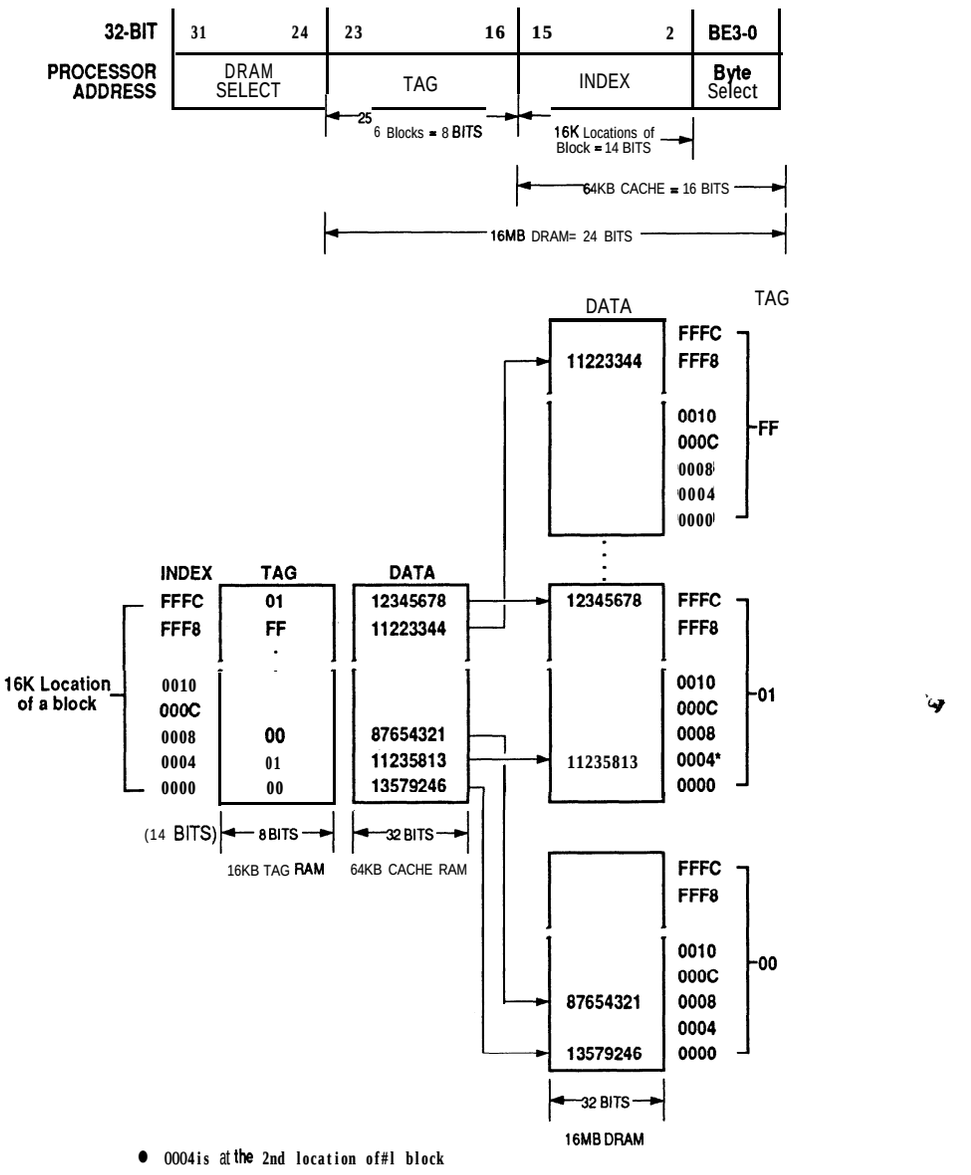


Figure: Direct-Mapped Cache Organization

The direct-mapped cache organization diagram above shows how data contained in cache are accessed.

For example, if the 80386 requests data at the address FFFFF9h in the main memory, the procedure is as follows:

- The cache-controlled logic determines the cache location from the 14 least significant bits of the index field (FFF8h).
- The cache controlled logic compares the tag field (FFh) with the tag stored at location FFF8h in the tag RAM.
- If the tag matches, the processor reads the second byte of the 4-byte sub-block from the data in the cache RAM.
- If the tag does not match, the cache logic fetches the 4-byte sub-block at address FFFFF8h in the main memory and loads it into location FFF8h of the cache RAM, replacing the current sub-block. The logic also changes the tag stored at locations FFF8h to FFh. The processor then reads the second byte of the new four-byte sub-block.

Cache Updating — Write-Back System

In a write-back system, the tag field of each block in the cache includes a bit called the ALTERED bit. The bit is set if the block has been written with new data and therefore contains data that is more recent than the corresponding data in the main memory. Before writing any block in the cache, the cache-controlled logic checks the altered bit. If it is set, the cache controlled logic writes the block to the main memory before loading new data into the cache.

The write-back system is faster than the write-through system because the number of times an altered block must be copied into the main memory is usually less than the number of write accesses.

Cache Coherency — Hardware Transparency

Write-Back eliminates stale data in the main memory caused by a cache-write operation. However, if a cache is used in a system in which more than one device has access to the main memory (a multi-processing system or a DMA system, for example), another stale data problem is introduced.

If new data is written to main memory by one device, the cache maintained by another device will contain stale data. A system that prevents the stale cache data problem is said to maintain cache coherency. The PEM-3301 uses the method of hardware transparency to maintain cache coherency.

Hardware ensures cache coherency by allowing all accesses to memory mapped by a cache to be seen by the cache. This is accomplished by routing the accesses of the all devices to the memory through the same cache.

The following figures show the cache memory organization and cache memory system implementation of the DTK PEM-3301.

Figure: Cache Architecture

Bus Width

The 80386 microprocessor supports two types of accesses: Memory, and Input/Output. Each type of access can be 32, 24, 16, or 8 bits wide. Memory and I/O devices can have paths 32, 16, or 8 bits wide. The PEM-3301 allows any type of access to a device of any width. If necessary, the hardware can break up a 80386 cycle into the required number of cycles(up to 32/8 = 4) to allow access to a 16 or 8 bit device.

All the onboard memory devices except the EPROM which contains the BIOS are organized into a 32-bit wide memory. These include the DRAM and the high-speed cache memory.

Memory Subsystem

In the IBM PC-AT, conventional memory or base memory extends from 0 to 640KB. This is the user area, and is available for use by application software.

Physical memory address space from 640KB to 1MB is reserved for the system.

DOS can recognize and use the memory area from 0 to 1MB only. Refer to the figure for the memory map on page 41.

One way of overcoming the 640KB barrier is by using expanded memory. This requires the use of additional bank-switched physical memory (memory organized in banks which can individually be switched on or off) along with LIM Expanded Memory Specification (EMS) compatible Expanded Memory Manager (EMM) software and an application program that is capable of working with the EMM software.

The EMM software first finds a 64KB page frame in the unused part of system memory, divides the frame into four 16KB windows and swaps in four 16KB pages from different areas of the additional physical memory. The Additional page memory used along with ah EMS emulator is known as Expanded Memory.

Applications programs (Netware and the XENIX operating system) can use physical memory beyond 1MB without the EMM manager. This additional memory is referred to as Extended Memory.

The PEM-3301 mainboard can have up to 8MB DRAM onboard with different types of DRAM in various configurations (refer to the Configuration section).

If necessary, the PEI-306 32-bit memory board can accomodate up to 16MB of system memory.

Unpacking the PEM-3301 Mainboard

This chapter will guide you through the physical installation of the PEM-3301 mainboard.

When you unpack and handle the board and other system components, all materials should be placed on a anti-static mat. You should wear an anti-static wristband connected to the same ground as the anti-static mat is.

Inside the carton, the mainboard is packed in an anti-static bag, and sandwiched between sheets of sponge. Take out the mainboard and place it on the grounded surface described above, with the component side up.

Inspect the mainboard for damage. Components mounted in sockets should be pressed down to ensure that they are properly seated. If any evidence of damage to the mainboard is apparent, do not turn on the power if the board is already installed or attempt to continue installation without obtaining authorized technical assistance.

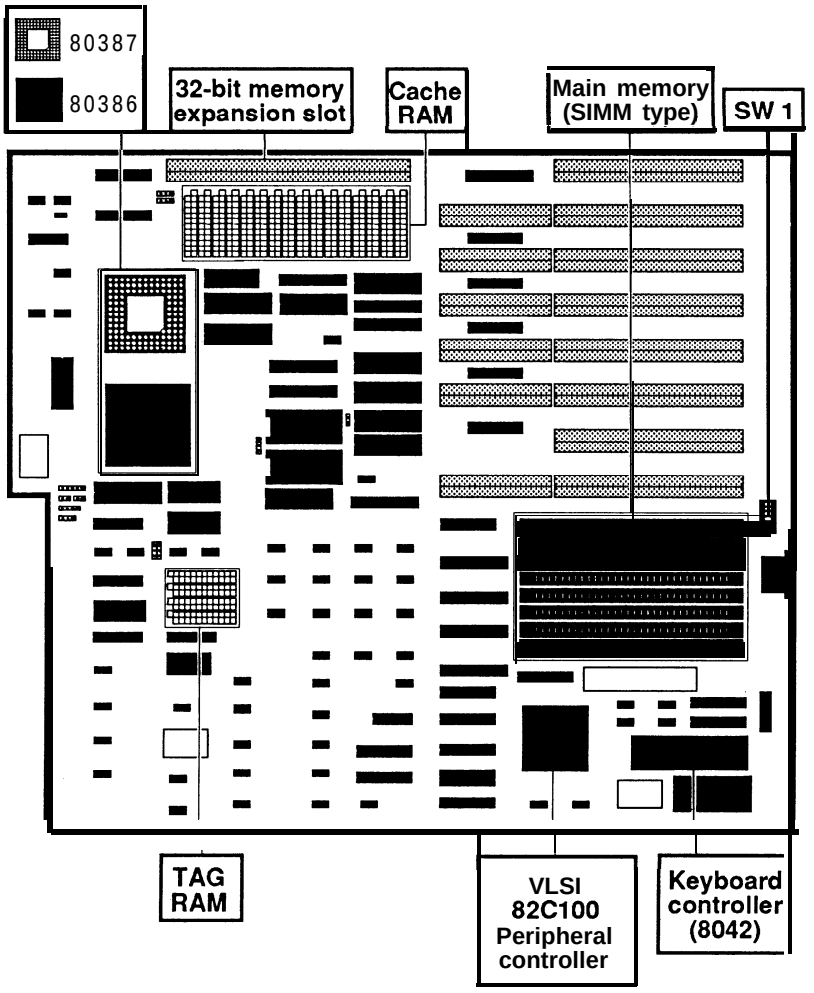
Restrict ions

Before installing the PEM-3301, we strongly recommend that you follow the restrictions mentioned below.

Access Time:

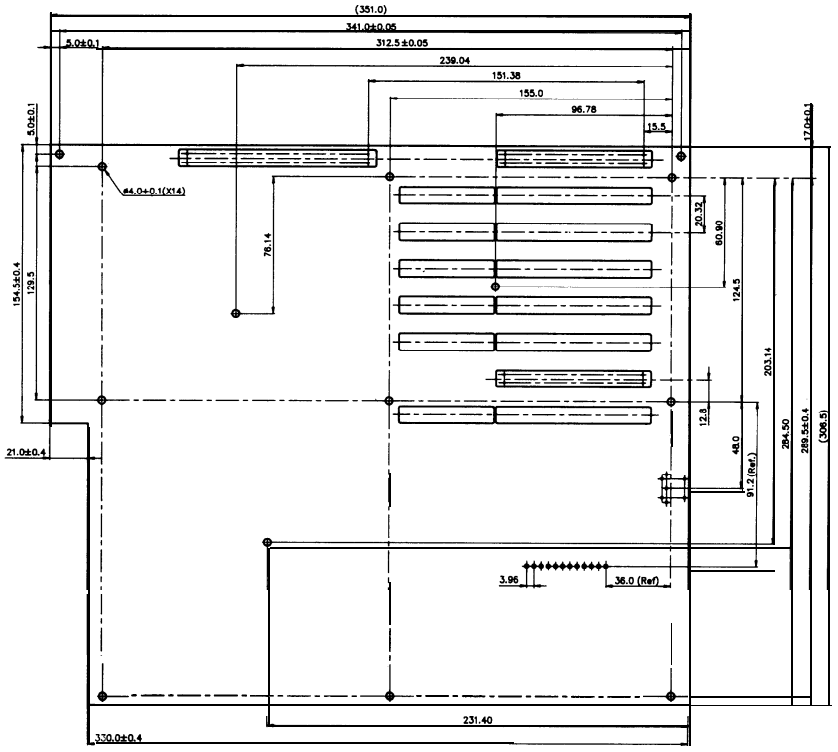
- *27256* EPROM (BIOS) with 150ns access time
- 1MbitX9 SIMM DRAM with 100ns access time
- 256KbitX9 SIMM DRAM with 80ns access time
- 16Kbit X *4* DIP Cache RAM (SRAM) with Data: 25ns, TAG: 15ns
- All the SIMM RAM modules must have leads

The figure below will familiarize you with the layout of the PEM-3301 Cache-386 33MHz Mainboard.



Dimensions of PEM-3301

All dimensions are in millimeter(s).



The PEM-3301 mainboard has two kinds of dual sockets for Cache RAM and one kind of SIMM socket for DRAM.

Chip Insertion

Remember that when inserting chips/RAM modules, you must make sure the notched or dotted end of the chip/RAM module is lined up with the notched end of the socket. Gently push the chip/RAM module into the socket, and be careful not to bend the pins. See the figures below:

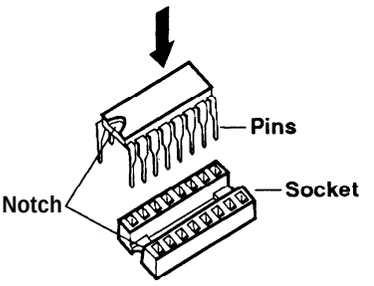


Figure: DIP-Type Cache RAM

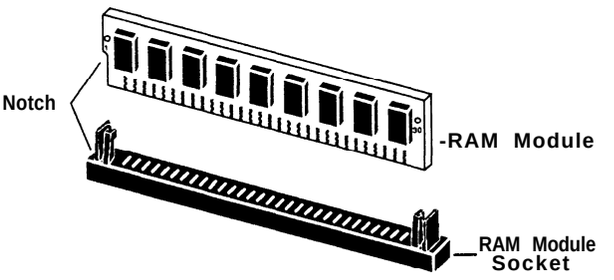


Figure: SIMM-Type DRAM

The location of the six-switch DIP SW1 can be seen below. Each switch has an ON and OFF position (usually the ON position is labeled, the OFF position is not). SW1 should be set appropriately, based on the following description.

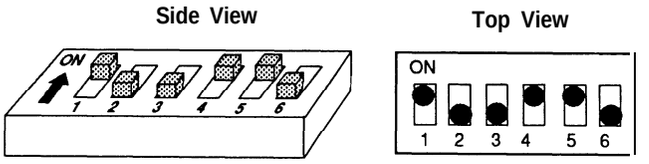


Figure: The Six-Switch DIP SW7

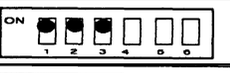
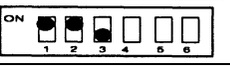
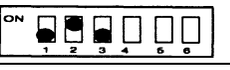
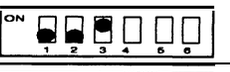
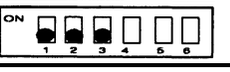
Memory Size	Switch SW1 (1 - 3)
2MB	
4MB	
8MB	
12MB	
16MB	

Table: Total 32-Bit Memory

Note: Total 32-bit memory means onboard 32-bit memory plus that on the PEI-306 32-bit extended memory card.

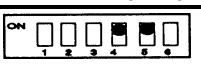
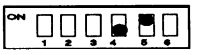
Memory Size (Bank 0, Bank 1)		Switch SW1 (4 - 5)
2MB	(1MB, 1MB)	
4MB	(4MB, OMB)	
5MB	(1 MB, 4MB)	
8MB	(4MB, 4MB)	

*Table: **Onboard 32-Bit** Memory*

Note:

- The switch setting of the onboard 32-bit memory must correspond to the physical memory installed onboard.
- The switch setting of the PEI-306 must correspond to the physical memory installed on the card.
- If you don't have a 16-bit memory extension card, the switch setting for total 32-bit memory must be for an amount larger than or equal to total installed memory (including onboard 32-bit memory and 32-bit memory on the PEI-306).

  For example, if the total memory installed is 8MB (4MB onboard and 4MB on the PEI-306), the switch setting for total 32-bit memory could be 8MB, 12MB or 16MB.

But if you use some other BIOS, with the switch settings (SWI-1, SW1-2, SWI-3) for total 32-bit memory larger than the physical DRAM installed, there will have an error message.

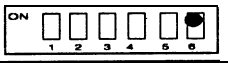
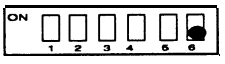
This is caused by different methods of testing memory among BIOSes. The solution is to set the switches for the total 32-bit memory in accordance with the physical DRAM installed. Most of the BIOSes do not have this problem.

- If you want to add a 16-bit extension memory card to the PEM-3301 mainboard, you have to fill the total 32-bit memory in accordance with the switch setting for total onboard 32-bit memory plus that on the PEI-306 32-bit extension memory card.

  For example, if the switch setting for total 32-bit memory is 6MB, you'll have to fill out the complete 6MB (5MB onboard and 1MB on the PEI-306 card or 4MB onboard and 2MB on the PEI-306 etc.) on the system before you can add a 16-bit extension memory card. Otherwise, there will be an address conflict for the memory.

Video Selection

The switch SWI-6 is used to select color or monochrome display modes. Refer to the figure below for the jumper settings.

Display Mode	Switch SW1 -6
Color	
Monochrome	

After the switches are set correctly, other attachments and jumper option adjustments on the mainboard have to be made. See the illustration below for the location of each of the jumpers and connectors. Most of the jumpers are preset at the factory.

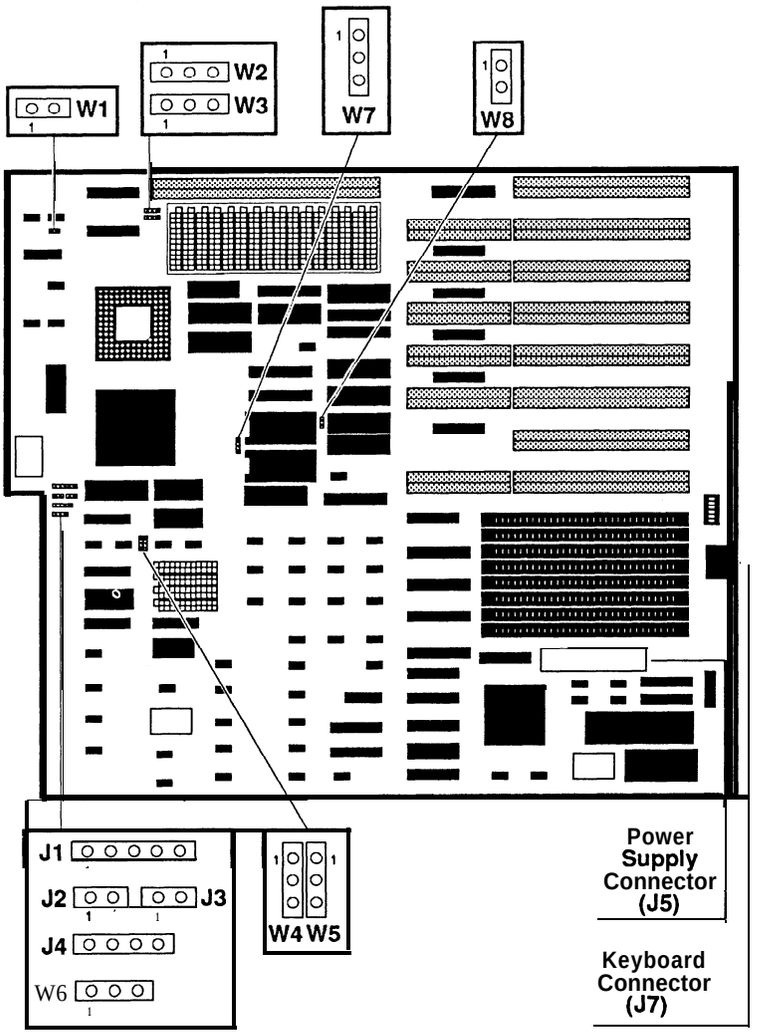
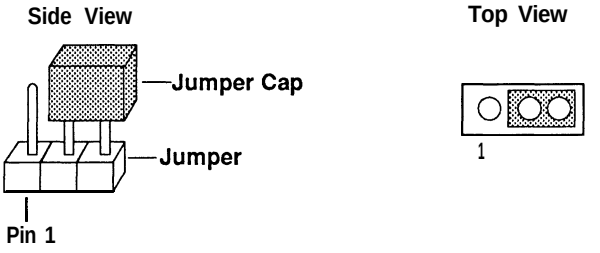


Figure: Location of Jumpers and Connectors

Jumper

A jumper is a kind of switch which uses a plastic cap with a metal interior to connect (short) two pins. If a jumper needs to be left open, you should save the cap for future use by covering one pin only of the jumper. This has no effect on the function of the board while it keeps the cap handy. The illustration below shows the side and top views of a three-pin jumper in which pins two and three are shorted.



With the mainboard oriented in the direction shown in the illustration above, the pins of each jumper are numbered from left to right in ascending order.

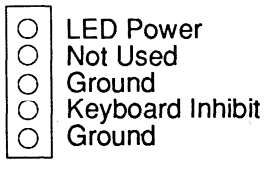
Functions of Connectors and Jumpers

A variety of connections can be made from the PEM-3301 mainboard to a control panel on the front of your system. Following is a brief explanation of the various functions of the connectors that PEM-3301 mainboard supports:

*Keyboard Lock/Power LED (Jumper **J1**)*

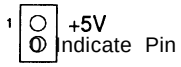
This connector connects the keyswitch to your control panel and also supplies the signal for the power LED. The pin assignments are listed below:

Jumper J1Pinouts



Turbo LED Connector (Jumper J2)

Jumper J2 is used to enable the Turbo LED. The Turbo LED in the hardware switch indicates operation in the Turbo mode.



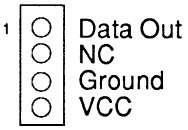
Reset Connector (Jumper J3)

This connector connects the reset switch to your control panel. If you encounter any problems while using unfamiliar software, you can always restart from the beginning by pressing the reset button. Note, however that any data which have not been saved to disk will be lost.

Jumper J3	Function
	Reset
	Default

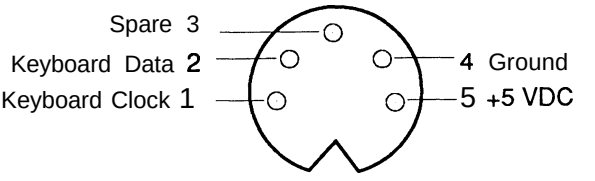
Speaker Connector (Jumper J4)

This connector uses only two lines for the speaker in the chassis. The pin assignments are:



Keyboard Connector (Jumper J7)

This connector may be located at the back of your system unit. Any AT-compatible keyboard with a 5-pin DIN connector may be used. The pin assignments for keyboard connector J7 are as follows:

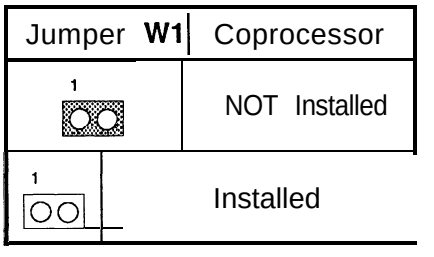


*Power Supply Connector (Jumper **J5)***

This connector is provided for the power supply. It is important that this connector be correctly connected; if not, the PEM-3301 board may be damaged. Information on connecting your power supply may be found in the "Connection to Power Supply" section.

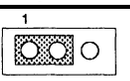
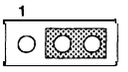
*Coprocessor Installation (Jumper **WI)***

Jumper **WI** is used to enable or disable the 80387 coprocessor. Refer to the figure below for jumper settings.



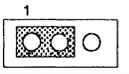
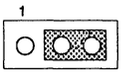
Bank 0 DRAM Type Selection (Jumper W2)

This jumper option allows you to set the DRAM type of bank 0 as either 1Mbit X *9* SIMM DRAM or 256Kbit X 9 SIMM DRAM.

Jumper W2	DRAM Type of the Bank 0
	(1Mbit x 9 SIMM DRAM)
	(256Kbit x 9 SIMM DRAM)

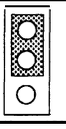
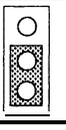
Bank7 DRAM Type Selection (Jumper W3)

This jumper option allows you to select the DRAM type of Bank 1 as either 1Mbit X 9 SIMM DRAM or 256Kbit X 9 SIMM DRAM.

Jumper W3	DRAM Type of the Bank 1
	(1 Mbit x 9 SIMM DRAM)
	(256Kbit x 9 SIMM DRAM)

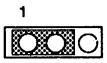
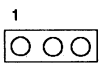
Cache Size Selection (Jumper W4- W5)

This jumper selects the various cache size configurations.

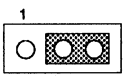
Jumper W4 - W5	Cache RAM Type
	64KB Cache Memory With 16Kbit x 4 SRAM Chip
	256KB Cache Memory With 64Kbit x 4 SRAM Chip

Turbo Connector (Jumper W6)

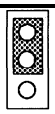
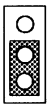
This connector switches the system between normal and turbo speeds.

Jumper W6	Hardware Method
	Normal, Emulate Without Cache Support
	Turbo, Cache Support in Ultra-High Speed

Note that Turbo and Normal modes can also be toggled with a software switch invoked from the keyboard as shown below:

JumperW6	Software Method
	Speed Toggled by Pressing <Ctrl>, <Alt> and <-> keys

EPROM Type Selection (Jumper W7)

Jumper W7	EPROM Type Selection
	For 27256
	For 27512

DMA Clock Speed Selection (Jumper W8)

Jumper W8	DMA Clock Speed Selection
	8MHz DMA
	4MHz DMA

Note: Some I/O cards which use DMA channel do not like high speed DMA **(8MHz DMA).** In this case, please change jumper W8 setting to low speed **DMA (4MHz** DMA).

Jumpers for Cache and Main Memory Configuration

The tables on page 27 indicate the jumper settings required for different SRAM cache configurations.

The cache configurations are listed below:

64KB: 64KB cache (with eight **16Kbit** x 4 cache SRAM chips and two **16Kbit** X 4 tag SRAM chips)

256KB: 256KB cache (with eight 64Kbit X 4 cache SRAM chips and two 64Kbit X 4 tag SRAM chips)

Refer to the next page for more information.

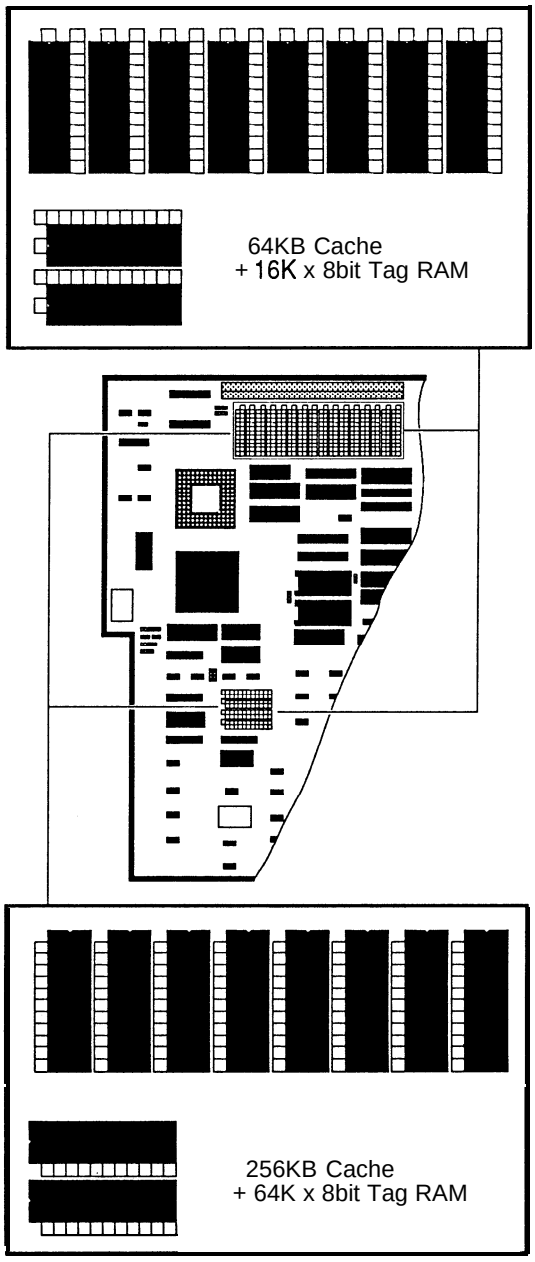
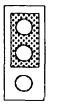
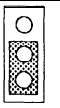


Figure: Cache Configurations

The following table lists the jumper settings required for each cache memory configuration listed above.

Jumpers W4 & W5	Cache Memory Configuration
	64KB
	256KB

The table on the next page shows the jumper and switch settings for different onboard memory (DRAM) configurations. Jumpers W2, W3 and switch SW1 are located on the mainboard.

To select the proper jumper setting for the RAM size that you want, refer to the figures on the following pages.

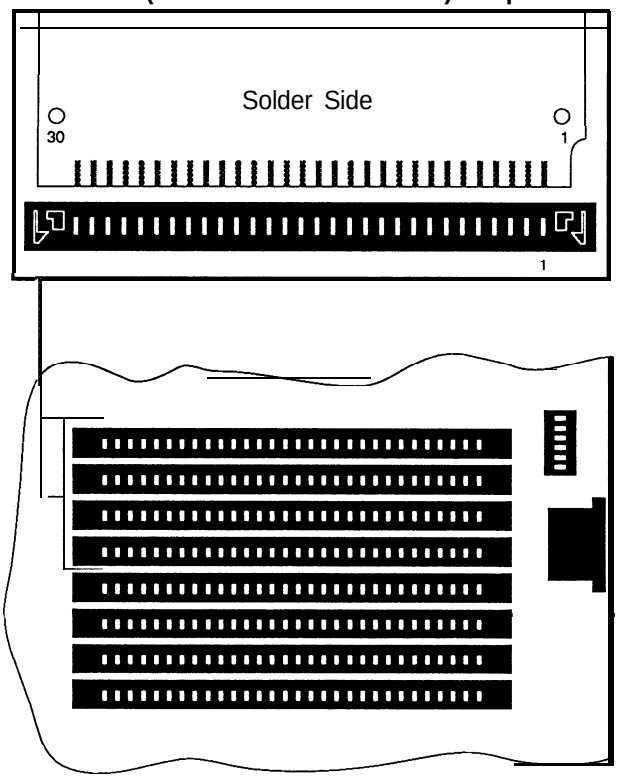
Two banks of main memory are on the PEM-3301, BANK 0 and BANK 1. Each bank acomodates the 32-bit wide data bus. BANK 0 must be installed first.

RAM SIZE	Onboard		Onboard Switch & Jumper settings			
	BANK 0	BANK 1	SW1	W2	W3	Reference
1MB	(256Kbit x 9) x 4 RAM Module	None				Page 29
2MB	(256Kbit x 9) x 4 RAM Module	(256Kbit x 9) x 4 RAM Module				Page 30
4MB	(1 Mbit x 9) x 4 RAM Module	None				Page 31
5MB	(256Kbit x 9) x 4 RAM Module	(1 Mbit x 9) x 4 RAM Module				Page 32
8MB	(1Mbit x 9) x 4 RAM Module	(1Mbit x 9) x 4 RAM Module				Page 33

Note : ■ means “ON” and ▫ means “OFF”

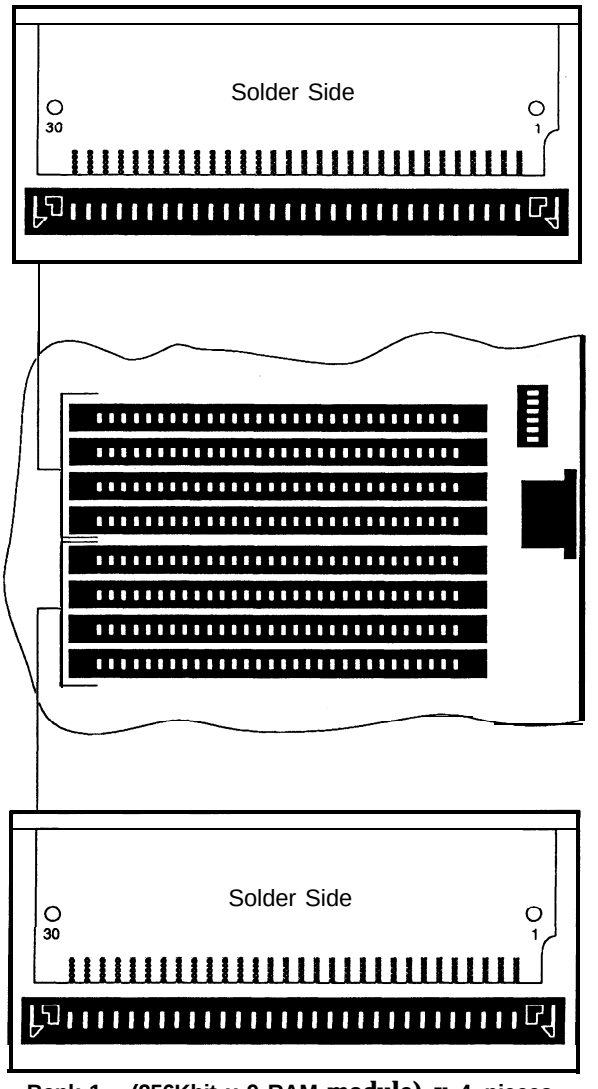
Table: DRAM Configurations

Bank 0 ▫ (256Kbit x 9 RAM module) x 4 pieces



2MB Total Onboard Memory

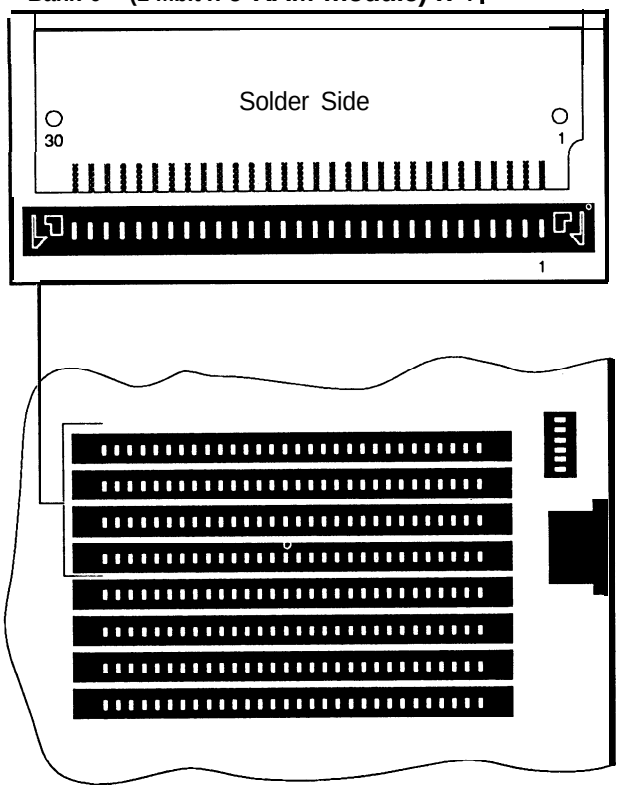
Bank 0 = (256Kbit x 9 RAM module) x 4 pieces



Bank 1 = (256Kbit x 9 RAM module) x 4 pieces

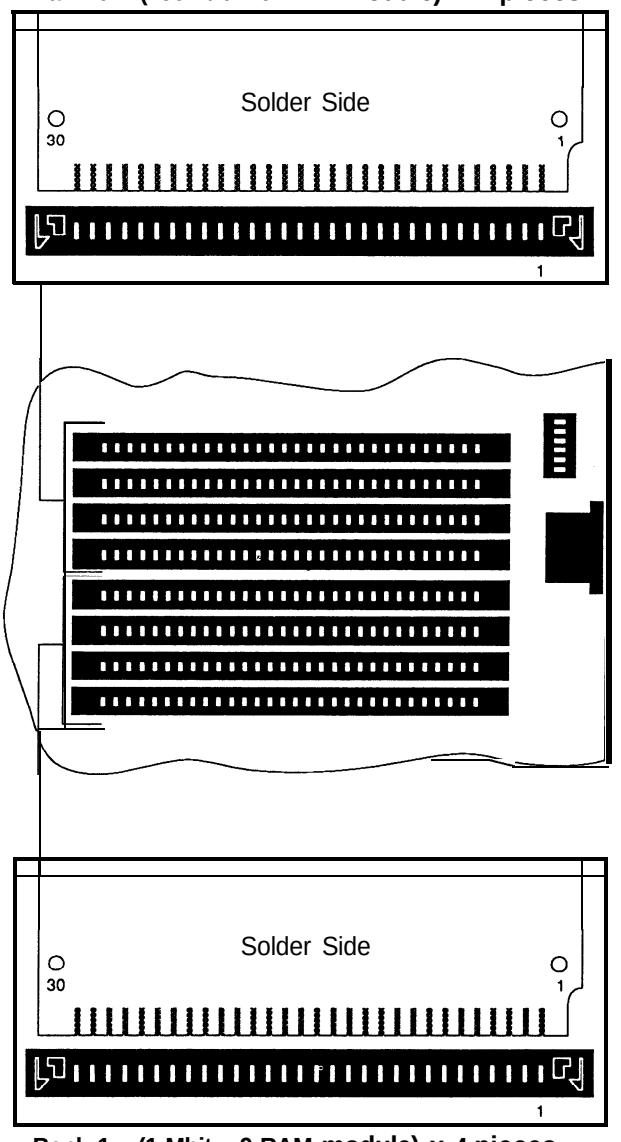
4MB Total Onboard Memory

Bank 0 = (1 Mbit x 9 RAM module) x 4 pieces



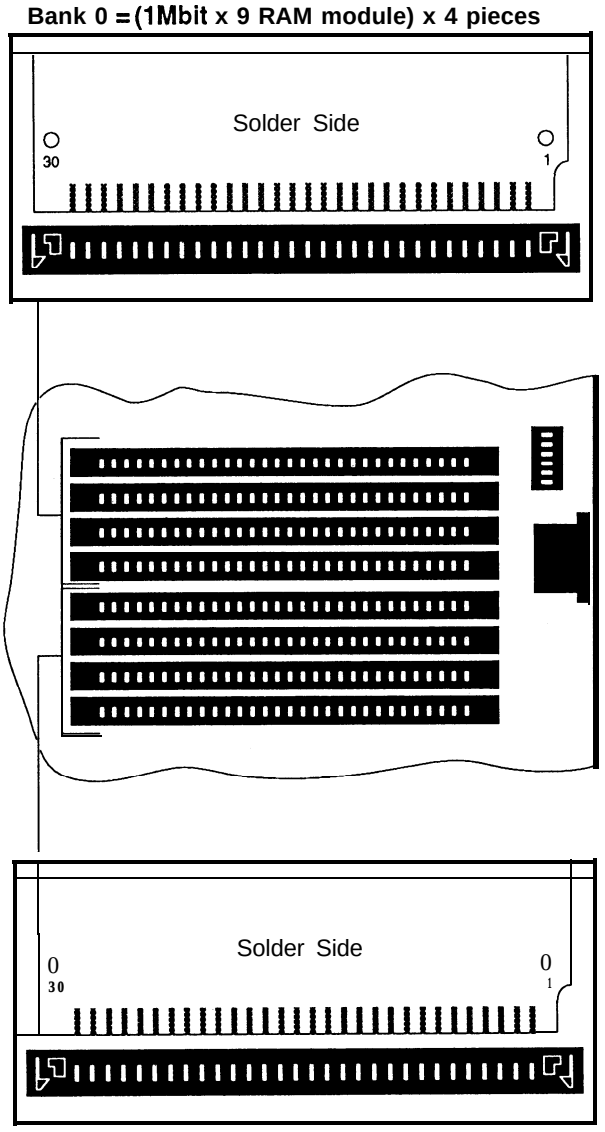
5MB Total Onboard Memory

Bank 0 = (256Kbit x 9 RAM module) x 4 pieces



Bank 1 = (1 Mbit x 9 RAM module) x 4 pieces

Bank 0 = (1Mbit x 9 RAM module) x 4 pieces



Bank 1 = (1Mbit x 9 RAM module) x 4 pieces

The PEM-3301 mainboard supports the Intel 80386-33 processor. The processor chip should be inserted into the processor socket(U12), with the notch as shown below.

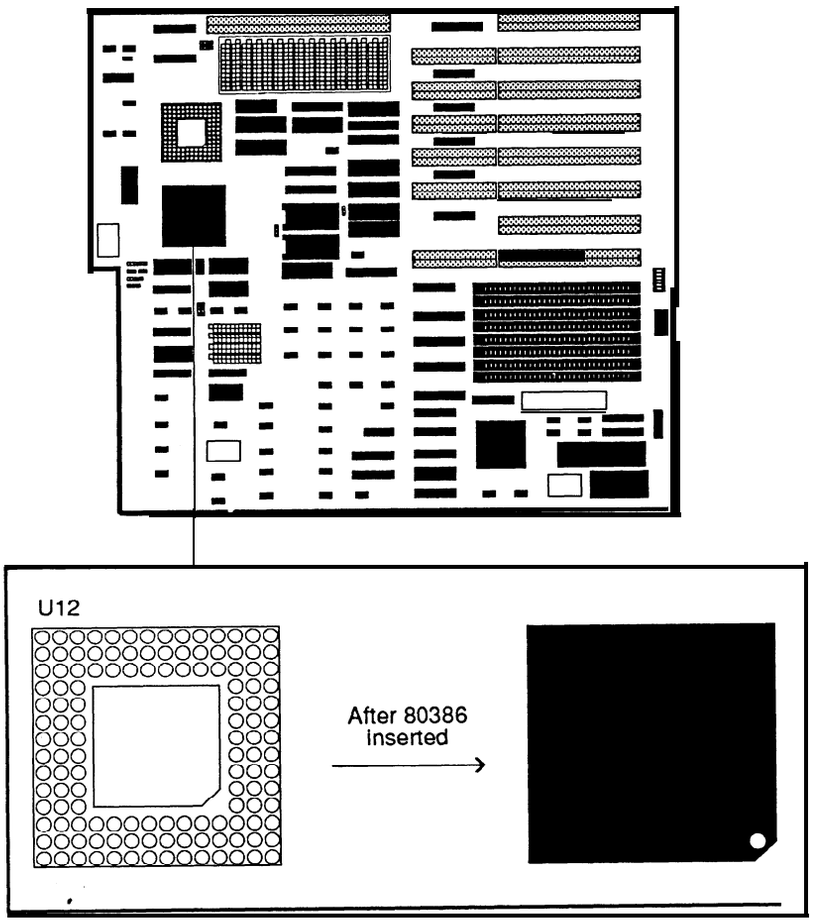


Figure.= Location of Processor

The PEM-3301 mainboard supports the Intel 80387 and Weitek 3167 numeric coprocessors. The coprocessor chip should be inserted into the coprocessor socket **(Ull),** with the notch on the package oriented in the same direction as the corresponding notch on the socket. The jumper WI should be SHORTED **if** an Intel 80387 or Weitek 3167 is not installed and OPENED if either one of them is installed. The position of the coprocessor sockets is shown below.

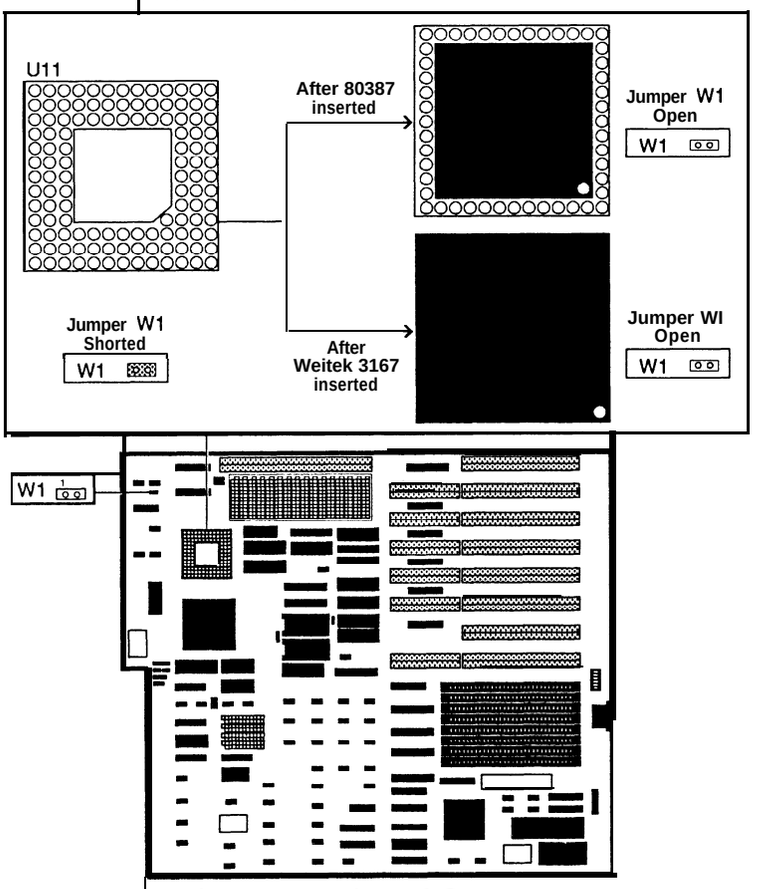
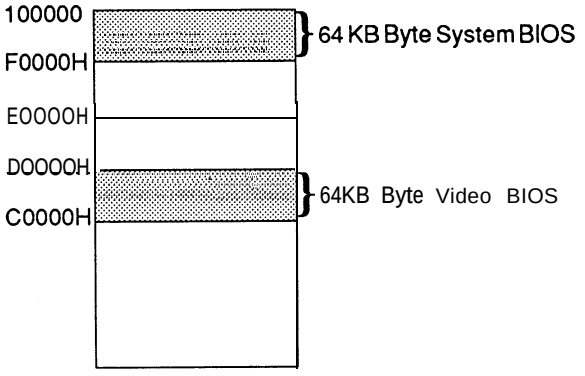


Figure: Location of ***Coprocessors***

For higher performance, the PEM-3301 has two shadow RAM functions. Shadow RAM is one of the features of the PEM-3301. Your BIOS or diskette will support the following:

- A 64KB DRAM space allocated for system BIOS shadow RAM
- A 64KB DRAM space allocated for video BIOS shadow RAM

BIOS and video addresses are allocated for shadow RAM. Both sections are 64KB in size. Refer to the table below for more information.



Note that a reserved 128K DRAM space is allocated for shadow RAM. You cannot use it for another purpose even if these functions are disabled. Refer to the Shadow RAM Control Port table below for more information.

I/O Port Address 72H		
Data bit 5	1	Shadow area write protect
	0	Shadow area write enable
Data bit 6	1	Enable video BIOS shadow
	0	Disable video BIOS shadow
Data bit 7	1	Enable system BIOS shadow
	0	Disable svstem BIOS shadow

If you use DTK or Phoenix 1 .1002 BIOS, you can enable or disable these two shadow RAM functions through your BIOS setup.

If your BIOS does not support shadow RAM, you may use the program on the diskette included with this mainboard to set up the shadow RAM driver. Follow the steps below:

- Insert the diskette into drive A and enter a:.
- Enter this command:
  SH_INST
- Respond to the prompts on your screen.

The shadow RAM utility is now installed. Your AUTOEXE.BATfile has been modified by the installation program. The shadow RAM function will automatically activate after you reboot your system.

If you want to update your shadow RAM utility, you may run the "SHADOW.EXE" file and modify shadow RAM as you desire.

Note:

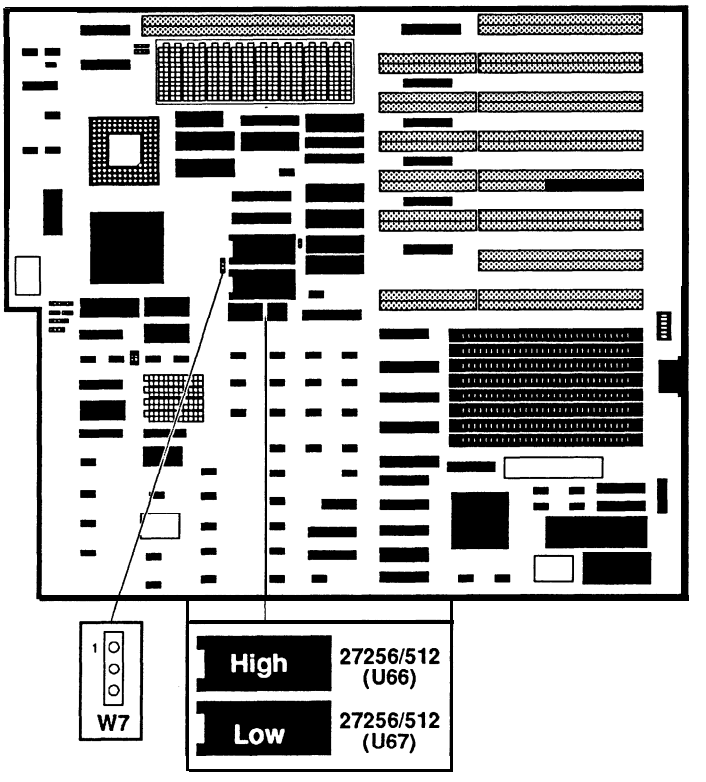
1. Because 128K of DRAM is reserved for shadow RAM, the switch setting for the starting address on the PEI-306 should be xMB + 256KB with x representing the onboard installed memory size.

2. If your adapter uses extended memory area as non-cacheable memory in the same way as dual-port memory, you have to locate the non-cacheable memory after the cacheable area is set by means of SW1-1 and SW1-2.

3. If your adapter BIOS is located at 0C8000H-OCFFFFH (within OCOOOOH-OCFFFFH) and cannot be cached, you should move the address to a non-cacheable area like ODOOOOH-ODFFFFH or disable video shadow function..

4. Cacheable area means physical 32-bit memory installed area and shadow RAM area (OFOOOOH — OFFFFFH, OCOOOOH — OCFFFFH) if installed.

To install the ROM chips, refer to the illustration below for the location of the DIP sockers and ROM selection jumper W7 on the mainboard.



Type of BIOS	Type of ROM chip	ROM Configuration	Jumper W7
DTK BIOS or any other of 64KB size	27256 x 2	U66 - High byte U67 - Low byte	1
Other BIOS of 128KB size	27512 x 2	U66 - High byte U67 - Low byte	1

ROM access time is 150ns.

Because of the large numbers of jumpers and options on the PEM-3301 board, it is best to start with the factory default settings and make experimental modifications from that point. The following table shows the factory default settings.

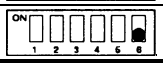
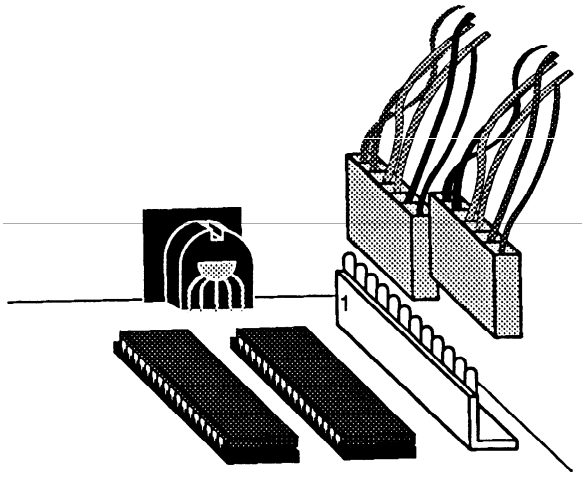
Jumper or Switch	Short or Switch	Function
W1		Coprocessor Not Installed
w2		256Kbit x 9 RAM Module as Bank 0
w3		256Kbit x 9 RAM Module as Bank 1
w4		64K Cache Memory
W5		64KCache Memory
W6		High Speed 33MHz
W7		For 27256
W8		8MHz DMA Clock
SW 1 --1 -5		Onboard 2MB Main Memory
SW1-6		Monochrome Display

Figure: Factory Default Settings

If you are installing the PEM-3301 yourself, the final step is attaching the power supply cable to the mainboard at connector J8, which is located in the upper right quadrant of the board. There are some cables on the power supply.

Be sure the four black wires of the power supply are located at the middle of the power connectors. Refer to the figure below. Pin 1 is shown in the picture for your convenience.



The pinouts for the connectors at J5 are as follows:

Pin	Assignment
1	Power Good
2	+5 VDC
3	+12 VDC
4	-12 VDC
5	Ground
6	Ground
7	Ground
8	Ground
9	-5 VDC
10	+5 VDC
11	+5 VDC
12	+5 VDC

Entering 33MHz Cache Mode

Software Switch

When pins 2 and 3 of jumper W6 are shorted, the system speed may be toggled between Turbo (cache support in ultra-high speed) and Normal (emulate without cache support in lower speed) by holding down the control <Ctrl> and alternate <Alt> keys on the keyboard while pressing the minus <-> key.

The Turbo LED on the front panel will light in Turbo mode.

Hardware Switch

When pins 1 and 2 of jumper W6 are connected by the switch on the control panel, push the hardware switch OFF to enter Turbo mode and push it ON to enter Normal mode. The Turbo LED will light in the Turbo mode.

System Memory Map

The AT-compatible system memory map is as follows:

Starting Address	Amount	Function
000000h	640KB	Primary DOS/Application Area
0A0000h	128KB	Used for graphics display buffers
0C0000h	128KB	Reserved for ROM
0E0000h	64KB	Onboard auxiliary ROM
OFOOOOh	64KB	System BIOS and BOOT ROM
100000h	15MB	AT compatible extended memory
FF0000h	64KB	Same as 0F0000h

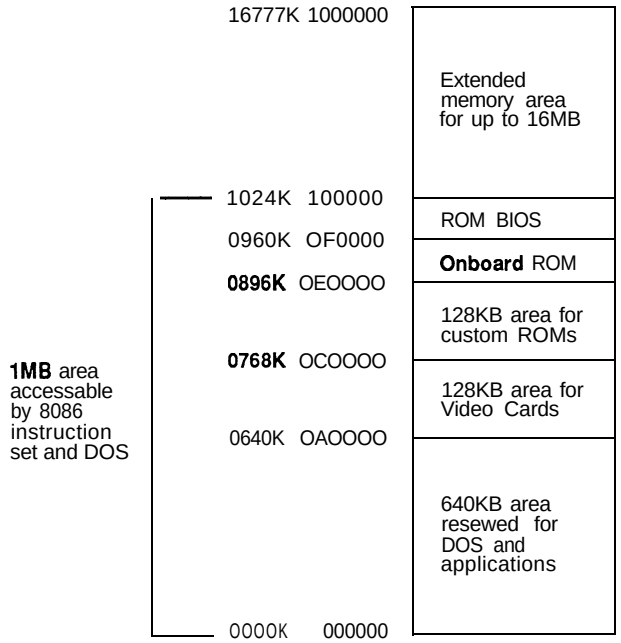


Figure: System Memory Map

There are three programmable timer/counters in the 8254 portion of the VLSI 82C100 chip. The three independent 16-bit counters and six software-programmable counter modes connect to system software

They appear as an array of four external I/O ports. Three ports are used as counters, and the fourth is a control register for mode programming. The timer channels are defined as channels 0, 1 and 2.

They are used as follows:

Channel 0	System Timer
GATE 0	TIED ON
CLK IN 0	1.190MHz OSC
CLK OUT 0	8259A IRQ 0

Channel 1	Refresh Request Generator
GATE 1	TIED ON
CLK IN 1	1.190MHz OSC
CLK OUT 1	Request Refresh Cycle

Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PP1 bit
CLK IN 2	1.190MHz OSC
CLK OUT 2	Used to drive speaker

The CPU may be interrupted by two 8259 Interrupt Controllers in the VLSI 82C100 as well as the NMI signal. This allows 16 levels of interrupt, each with its own level of priority. Any interrupt including NMI can be disabled. The following table shows the interrupt level assignments.

Level	Function
NMI	Mainboard memory parity or I/O channel check

Interrupt Controllers

Level	Function
Microprocessor NMI	Parity or I/O Channel Check
Interrupt Controllers	
CTLR1 CTLR2	
IRQO	Timer Output 0
IRQ 1	Keyboard (Output Buffer Full)
IRQ 2	Interrupt from CTLR 2
IRQ 8	Realtime Clock Interrupt
IRQ 9	Software Redirected to INT OAH (IRQ2)
IRQ 10	Reserved
IRQ 11	Reserved
IRQ 1'2	Reserved
IRQ 13	Coprocessor
IRQ 14	Fixed Disk Controller
IRQ 15	Reserved
IRQ 3	Serial Port 2
IRQ 4	Serial Port I
IRQ 5	Parallel Port 2
IRQ 6	Diskette Controller
IRQ 7	Parallel Port 1

DMA Channels

The PEM-3301 mainboard supports up to seven DMA channels. Two 8237 DMA controllers are in the VLSI 82C100 chip. Each 8237 has four DMA channels. DMA controller 1 has channel 0 through channel 3 and DMA controller 2 contains channel 4 through channel 7. Channel 4 of controller 2 is used to cascade the four channels of the controller 1, namely, channel 0 through channel 3, to the microprocessor. DMA channel assignments are listed below:

CTR 1		CTR 2	
CH 0	Spare	CH 4	Cascade for CTRL 1
CH 1	SDLC	CH 5	Spare
CH2	Diskette	CH6	Spare
CH 3	Spare	CH 7	Spare

The channels of DMA Controller 1 support data transfers between 8-bit I/O adapters and 8-bit or 16-bit system memory, and the channels of DMA Controller 2 are used for 16-bit data transfers between 16-bit I/O adapters and 16-bit system memory.

I/O Channel

This section describes the I/O channel, lists the pin assignments, describes each I/O channel signal line and gives the I/O address map.

The I/O channel has the following features:

- I/O address space from 100h to 3FFh
- Selection of data accesses (8-bit or 16-bit)
- 16MB memory address space
- 11 levels of interrupt
- 7 DMA channels

- Open-bus structure (allowing multiple microprocessors to share system resources, including system memory)
- Refresh of system memory by the system microprocessor
- There are six 16-bit adapter (one 62-pin and one 36-pin connector) slots, two 8-bit adapter (one 62-pin connector) slots, and one 32-bit memory board (80-pin connector) slot.

The following illustration shows the pin assignments of the I/O channel connectors.

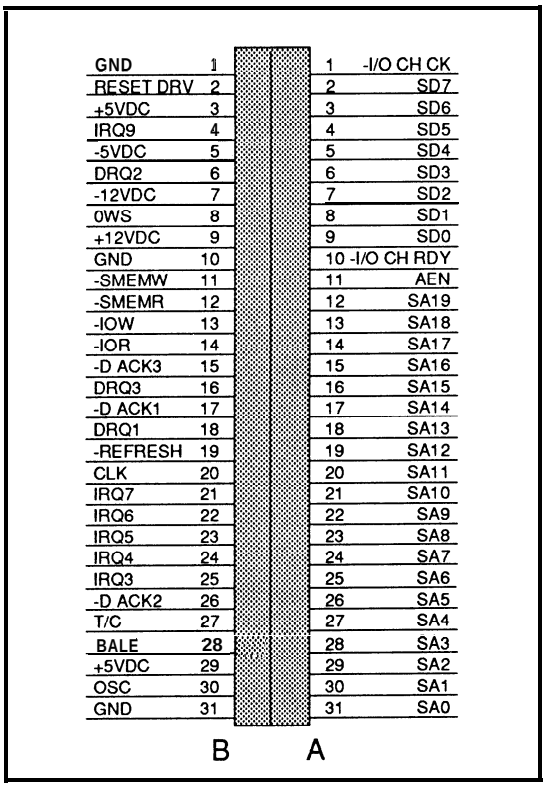


*Figure: Sixty-Two Pin **I/O** Channels*

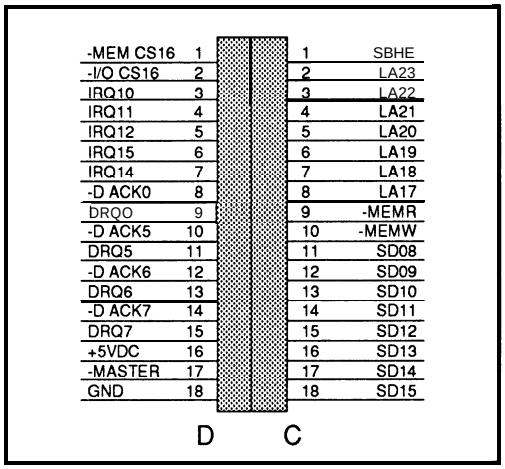


Figure: Thirty-Six Pin I/O Channels

I/O Channel Signal Description

The following is a description of the system board's I/O channel signals. All signal lines are TTL-compatible, I/O adapters should be designed with a maximum of two low-power Shottky(LS) loads per line.

SAO Though SA79 (I/O)

Address bits 0 though 9 are used to address memory and I/O devices within the system. These 20 address lines, in addition to LA17 through LA23, allow access of up to 16Mb of memory. SAO through SA19 are gated on the system bus when "BALE" is high and are latched on the falling edge of "BALE". These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

LA17 Through LA23 (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16 MB of addressability. These signals are valid when "BALE" is high. LA17 through LA23 are not latched during microprocessor cycles and therefore do not stay vaild for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of "BALE". These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

CLK (0)

This is the 8.25MHz system clock with a cycle time of 121 nanoseconds. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

RESET DRV (0)

"Reset drive" is used to reset or initialize system logic at power-up time or during a low line voltage outage. This signal is active high.

SD0 Through SD15 (I/O)

These signals provide bus bits 0 though 15 for the microprocessor, memory, and I/O devices. DO is the least-significant bit and D15 is the most significant bit.. All 8-bit devices on the I/O channel should use DO through D7 for communications to the microprocessor. The 16-bit devices will use DO through D15. To support 8-bit devices, the data on D8 through D15 will be gated to DO through D7 during 8-bit transfers to these devices: 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

BALE (0) (Buffered)

"Address latch enable" is provided by the 82288 Bus Controller and is used on the system board to latch

valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with "'AN""). Microprocessor addresses SAO through SA19 are latched with the falling edge of "BALE" "BALE" is forced high during DMA cycles.

-I/O CH CK (I)

-I/O channel check provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

I/O CH RDY (I)

"I/O channel ready" is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its vaild address and a Read or Write command. Machine cycles are extended by an integral number of clock cycle (167 nanoseconds). This signal should be held low for no more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 and IRQ 14 through 15 (I)

Interrupt Requests 3 through 7, 9 through 12, and 14 though 15 are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). Interrupt 13 is used on the system board and is not available on the I/O channel. Interrupt 8 is used for the real-time clock.

-IOR (I/O)

"-I/O Read" instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

-10 w (I/O)

"-I/O Write" instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

-SMEMR (O) -MEMR(I/O)

These signals instruct the memory devices to drive data onto the data bus. "-SMEMR" is active only when the memory decode is within the low 1Mb of memory space. "-MEMR" is active on all memory read cycles. "-MEMR" may be drven by any microprocessor or DMA controller in the system. "-SMEMR" is derived from "MEMR" and the decode of the low 1Mb of memory. When a microprocessor on the I/O channel wishes to drive "-MEMR", it must have the address lines valid on the bus for one system clock period before driving "-MEMR" active. Both signals are active LOW.

-SMEMW (0) -MEMW (l/0)

These signals instruct the memory devices to store the data present on the data bus. "-SMEMW" is active only when the memory decode is within the low 1Mb of the memory space. "-MEMW" is active on all memory read cycle. "-MEMW" may be driven by any microprocessor or DMA controller in the system. "-SMEMW" is derived from "-MEMW" and the decode of the low 1 Mb of memory. When a microprocessor on the I/O channel wishes to drive "-MEMW", it must have the address lines valid on the bus for one system clock period before driving "-MEMW" active. Both signals are active low.

DRQO-DRQ3 and DRQ5-DRQ7 (I)

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel micreprocessors to gain DMA service (or control of the system). They are prioritized, with “DRQO” having the highest priority and "DRQ7" having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding “DMA Request Acknowledge” (DACK) line goes active. “DRQO” through "DRQ3" will perform 8-bit DMA transfers; "DRQ5" through "DRQ7" will perform 16-bit transfers. "DRQ4" is used on the system board and is not available on the I/O channel.

-DACK0 to -DACK3 and -DACK5 to -DACK7 (0)

-DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQO through DRQ7). They are active low.

AEN (0)

“Address Enable” is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and l/O), and the Write command lines (memory and I/O)

-REFRESH (I/O)

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

T/C (0)

“Terminal Count” provides a pulse when the terminal count for any DMA channel is reached.

SBHE (I/O)

“Bus High Enable” (system) indicates a transfer of data on the upper byte of the data bus, SD8 through

SD15. Sixteen-bit devices use "SBHE" to condition data bus buffers tied to SD8 though SD15.

-MASTER (I'

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a "-DACK". Upon receiving the "-DACK", an I/O microprocessor may pull "-MASTER" low, which will allow it to control the system address, data, and control lines (a condition known as tri-state): After "-MASTER" is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, two clock periods before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

-MEM CS16 (I)

"-MEM 16 Chip Select" signals the system board whether the present data transfer is a 1 wait-state, 16-bit, memory cycle. It must be derived from the decode of LA17 through LA23. "-MEM CS16" should be driven with an open collector or tri-state driver capable of sinking 20 mA.

osc (0)

"Oscillator" (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

ows (I)

The "Zero Wait State" (OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, "0WS" is derived from an address decode

gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, "0WS" should be driven active one system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. "OWS" is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

I/O Address Map

The I/O address map of the PEM-3301 is given below. Note that the I/O addresses from hex 000 to hex OFF are reserved for the mainboard, and the addresses from hex 100 to hex 3FF are available on the AT I/O bus.

Address Range	Device
000-01 F	DMA Controller 1, 8237
020-03F	Master Interrupt Controller, 8259
040-05F	Timer, 8254
060-06F	Keyboard Controller, 8042
070-07F	Real-time clock, NMI mask
080-09F	DMA Page Register,74LS612
OAO-OBF	Interrupt Controller2, 8259
OCO-ODF	DMA Controller 2, 8237
0F0	Clear Math Coprocessor Busy
OF1	Reset Math Coprocessor
0F8-OFF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31 F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3C F	Enhanced Graphics Display Adapter
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

The keyboard controller is based on the 8042(U128) single-chip microprocessor and is used to support the PEM-3301 keyboard interface. The keyboard controller performs the following functions:

- Receives serial data from keyboard, checks parity, translates it into a system scan code, if necessary, transfers data to the data buffer and interrupts the processor.
- Executes system commands, places the results in the data buffer and interrupts the processor if necessary.
- Transmits the system data in the data buffer to the keyboard in the serial format along with the parity bit. Reports the response of the keyboard to the system.
- Reports errors to the system through the status register.

The keyboard controller has two 8-bit ports. One of them serves as an input port, while the other serves as an output port. Besides these, there are two test inputs. One of them, namely TESTO, is used to monitor the state of the clock line, while the other, namely TEST1, is used to read the state of the keyboard's data line.

Input Port Bit	Definition
Pin 27 - Bit 0	Undefined
Pin 28 - Bit 1	Undefined
Pin 29 - Bit 2	Undefined
Pin 30 - Bit 3	Undefined
Pin 31 - Bit 4	Undefined
Pin 32 - Bit 5	Undefined
Pin 33 - Bit 6	Undefined
Pin 34 - Bit 7	Keyboard Inhibit Switch 0 Inhibited 1 Not inhibited

Output Port Bit	Definition
Pin 21 - Bit 0	System Reset
Pin 22 - Bit 1	Gate A20 of system processor 0 A20 inhibited 1 A20 Not inhibited
Pin 23 - Bit 2	Undefined
Pin 24 - Bit 3	System speed selection 0 Normal 133MHz, Turbo
Pin 35 - Bit 4	Output buffer full 0 Not full 1 Full (IRQ1)
Pin 36 - Bit 5	Undefined
Pin 37 - Bit 6	Keyboard clock (output)
Pin 38 - Bit 7	Keyboard data (output)

32-Bit Memory Expansion Bus

The 32-bit memory expansion bus optimizes the memory subsystem to take advantage of the 32-bit architecture of the 80386. This bus is not intended to be a general-purpose, industry-standard of the 32-bit expansion bus. It is simply a mechanism to optimize the performance of the PEM-3301 memory subsystem for the 80386 architecture.

The following table shows the pin assignments of the 32-bit memory expansion bus.

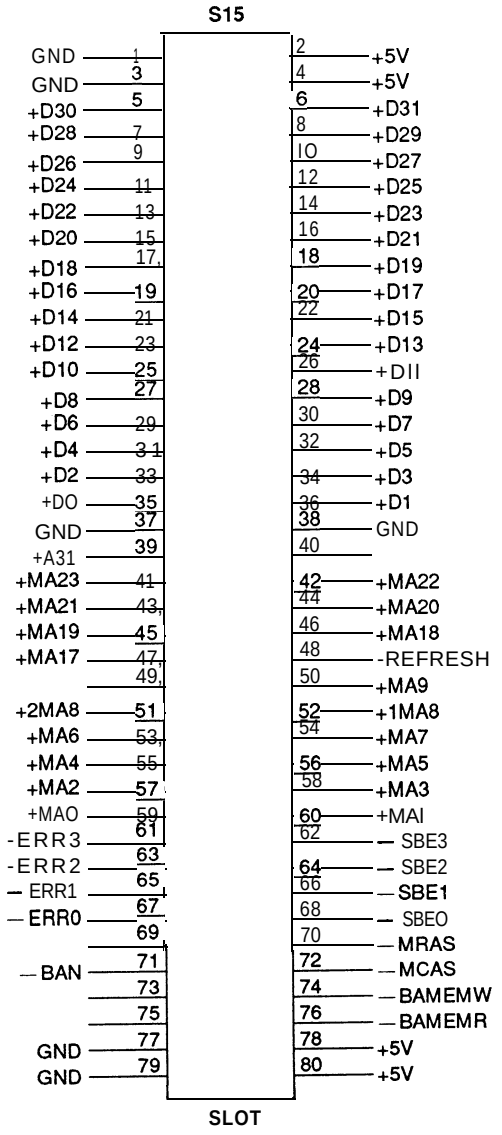


*Figure: Pin Assignments of the **32-Bit** Memory Expansion Bus*

Appendix A

Quick Reference for Jumper Settings

J1 — Keyboard Lock/ Power LED

J2 — Turbo LED Connector

J3 — Reset Connector

J4 — Speaker Connector

J5 — Power Supply Connector

J7 — ***Keyboard Connector***

W1 — Coprocessor Installation

W2 — Bank 0 DRAM Type Selection

W3 — DRAM Type of the Bank 7

W4- W5 — ***Cache Size Selection***

W6 — Turbo Connector

W7 — EPROM Type Selection

W8 — DMA Clock Speed Selectio